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ÊNIO COSTA RESENDE

ANTI-ISLANDING ALGORITHM BASED ON ACTIVE PHASE JUMP WITH POSITIVE FEEDBACK AND INTERMITTENT PERTURBATION FOR INTEGRATION OF INVERTER-BASED DISTRIBUTED ENERGY RESOURCES TO THE ELECTRIC POWER SYSTEM

UFU

2024

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Doctoral thesis submitted to the PostGraduate Program in Electrical Engineering at the Federal University of Uberlândia in partial fulfillment of the requirements for the degree of Doctor of Sciences.

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To Marina Pires dos Santos.

To Maria Eleuza Alves dos Santos (in memoriam)

To Antonio Tarcísio Bernardes (in memoriam)

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ÊNIO COSTA RESENDE

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To God!

“This is our island. It's a good island. Until the grownups come to fetch us we'll have fun.”

— William Golding, Lord of the Flies

Abstract

The growing penetration of Distributed Generation Systems (DGS) based on renewable resources into the distribution utility grid paves the way for a new energy generation and for an electrical consumption paradigm founded on the gradual replacing of fossil fuels by clean power generation. However, in spite of all its benefits, the adoption of the DGS brings new problems and challenges that must be addressed by the academical research. One of the main security issues is the unintentional islanding. Defined as the loss of the connection with the main grid, the unintentional islanding phenomenon can lead to the increasing of the harmonic pollution of the grid, electrical accidents with maintenance workers and out-of-phase reclosures. The purpose of this work is to present a new Anti-Islanding Protection (AIP) algorithm, based on the insertion of a phase jump at the beginning of each half cycle of the inverter output current. This phase jump will be parametrized with a positive frequency feedback in order to improve the algorithm performance by linking the frequency error with the inserted disturbance. Futhermore, the new AIP scheme defines maximum and minimum frequency alarm thresholds that, when reached, trip an additional phase jump to improve islanding detection, reducing the detection time and mitigating the Non-Detection Zone (NDZ) without demanding extra current harmonic degradation. Beyond this, the work also performs a complete review of the islanding theory, addressing the NDZ concept and its mapping technologies and conducting a critical analysis of the already existing solutions, highlighting the evolution timeline of each algorithm. Finally, in order to attest the new solution effectivity, it will be also carried out a comparative study with other already known AIP methods: Active Frequency Drift (AFD), AFD by (CHEN et al., 2013), AFD with Pulsating Chopping Factor (AFDPCF), Sandia Frequency Shift (SFS) and the Active Phase Jump with Positive Feedback (APJPF). The test methodology will be based on the most restrictive Standards recommendations and the results will be categorized according to three Key Parameter Indicators (KPI): detection time, NDZ and THDi. The obtained results show that the proposed scheme reached the mitigation of the NDZ and accomplished the fastest islanding detection for all of the tested cases.

Keywords: *Anti-Islanding, Distributed Generation, Grid Tied Photovoltaic Systems, Non-Detection Zone, Time Detection.*

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SUMMARY

Nomenclature

ABNT	Brazilian Association of Standards
AC	Alternate Current
AFD	Active Frequency Drift
AFDPCF	Active Frequency Drift with Pulsating Chopping Factor
AIP	Anti-Islanding Protection
ANEEL	National Agency of Electrical Energy
ANSI	American National Standards Institute
APJPF	Active Phase Jump with Positive Feedback
APJPFIP	Active Phase Jump with Positive Feedback and Intermittent Perturbation
APS	Automatic Phase Shift
CEMIG	Companhia Energética de Minas Gerais
CIGRE	International Council on Large Electric Systems
DC	Direct Current
DG	Distributed Generation
DGS	Distributed Generation System
DTT	Direct Transfer Trip
FB	Filtering Block
GTPS	Grid-Tie Photovoltaics Systems
HD	Harmonic Distortion
IAFD	Improved Active Frequency Drift
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MSVS	Modified Sandia Voltage Shift
NBR	Brazilian Standard
NDZ	Non-Detection Zone
OUF	Over/Under Frequency
OUV	Over/Under Voltage
PCC	Point of Common Coupling
PD	Phase Detector
PID	Passive Islanding Detection
PJ	Phase Jump
PLCC	Power Line Carrier Communication
PLL	Phase Locked Loop
PR	Proportional Resonant
PRODIST	Distribution Procedures
PV	Photovoltaics
R	Receiver
ROCOF	Rate of Change of Frequency

ROCOFoP	Rate of Change of Frequency over Power
ROCOP	Rate of Change of Power
ROCORP	Rate of Change of Reactive Power
ROCOV	Rate of Change of Voltage
ROCPAD	Rate of Change of Phase of Angle Difference
RPV	Reactive Power Variation
SMS	Slip Mode Shift
SOGI	Second Order Generalized Integrator
SVS	Sandia Voltage Shift
T	Transmitter
THD	Total Harmonic Distortion
THDi	Total Harmonic Distortion of Current
THDv	Total Harmonic Distortion of Voltage
VCO	Voltage Controlled Oscillator
ZCD	Zero Crossing Detector

CHAPTER I

Distributed Generation and Islanding

1.1 Introduction

The integration of renewable resources can occur through large electrical centers or decentralized small-to-medium power plants located near consumers and local loads. The main advantages of the latter approach are the reduction of transmission power losses, the increased reliability of the electrical system, and the expansion of the energy matrix. However, the growing penetration of renewable-based Distributed Generation Systems (DGS) introduces new challenges and concerns regarding power quality and electrical safety. Some of the main issues are unsynchronized reclosing, malfunction of protection schemes, voltage regulation, and islanding (SHAFIQUE et al., 2021).

The islanding phenomenon is defined as the operation of a DGS without an electrical connection to the utility grid. It can occur as either a planned or unplanned contingency. While intentional islanding is a useful tool to ensure power for isolated areas or war-affected regions, unintentional islanding has no positive aspects and can lead to severe consequences for local loads, power converters, workers, and users of the electrical system. Thus, the main objective of this work is to provide the theoretical foundation for understanding the islanding phenomenon, the main causes and consequences of unintentional grid disconnection, and, finally, to present a new Anti-Islanding Protection (AIP) strategy based on positive frequency feedback and intermittent perturbation.

The work is structured as follow: Chapter I will present the concepts of Distributed Generation (DG) and unplanned islanding, beyond to highlight the main goals of this PhD thesis; Chapter II will conduct a minor review about the Grid-Tie Photovoltaics Systems (GTPS) and other ancillary themes for the understanding of the islanding phenomenon, especially in the GTPS context; Chapter III will perform a complete review of the AIP strategies, categorizing them as remote, local passive and local active schemes and present the proposed new AIP algorithm; Chapter IV will present the computational results of a comparative study between the proposed AIP scheme with other well-known anti-islanding methods; Chapter V will present the real-time implementation of the proposed method and will evaluate its capabilities of working in single inverter based DGS and in multi-DG environment; Chapter VI will present the main conclusions of this work.

1.2 Distributed Generation and Unplanned Islanding

Distributed Generation (DG) can be understood as the generation of electrical power near local loads, reducing the demand on large electricity generation centers. The literature, however, does not present a universal definition (ACKERMANN; ANDERSON; SODER, 2001), leading to inconsistencies among different interpretations.

(BHADORIA; PAL; SHRIVASTAVA, 2013) offers a review of various DG definitions. The IEEE describes DG as power generation small enough to be situated near the end user. The IEA defines it as any power generation unit that supplies power locally at the distribution voltage level, while CIGRE characterizes DG as any unit below 50 MW connected to the distribution grid without centralized planning. In Brazil, ANEEL's Normative Resolution 482 from April 17, 2012, specifies the legal requirements for connecting distributed generation to the distribution grid, also differentiating between micro and mini generation (ANEEL, 2012).

- Distributed Microgeneration: power generation systems with installed capacity equal or inferior to 75 kW. This system, by its time, must present cogeneration or renewable resources.
- Distributed Mini generation: power generation systems with installed capacity in the range of 75 kW and 3 MW for disputable sources. For system with the presence of intermittent resources, this limit is relaxed to 5 MW.

The primary benefit of implementing Distributed Generation (DG) is its lower cost compared to centralized power plants. Additionally, Distributed Generation Systems (DGS) reduce transmission and distribution losses by generating power closer to end users. However, the adoption of DGS brings challenges, particularly in terms of the complexity of energy sector planning and security. A significant security concern is the issue of unintentional islanding.

The IEEE (2000) defines unintentional islanding as a condition where a DGS continues supplying power to a section of the electrical grid following an unexpected disconnection. This phenomenon can arise from unplanned distribution grid outages, scheduled disconnections for maintenance, human error, or sabotage. Its primary consequences include safety risks for users and utility workers, degradation in power quality, and risks related to out-of-phase reclosers. The next section will present regulations and recommendations on islanding and outline this work's general and specific objectives.

1.3 Islanding: Regulamentations and Recommendations

The Distribution Procedures (PRODIST), created by ANEEL, are technical guidelines governing access to the distribution grid and specifying quality and protective requirements for national systems. PRODIST comprises nine modules, with the third detailing requirements for integrating consumer generation systems with the main grid. Key standards for grid-connected Distributed Generation Systems (DGS) include protections for over/undervoltage, over/underfrequency, synchronization mechanisms, physical disconnection switches, and unintentional islanding prevention. While disconnection switches are required, other protections may be hardware-based or embedded in inverter algorithms. According to (CEMIG, 2012), DGSs using switched converters must meet ABNT NBR 16149 standards, which outline 14 safety and quality criteria necessary for inverter certification, aligned with ABNT NBR 16149, ABNT NBR 16150, and ABNT NBR IEC 62116 standards.

National standards like (ABNT, 16149) provide recommendations for DGS connections to the main grid. Meanwhile, (ABNT 16150) defines testing procedures to ensure devices interfacing between the DGS and distribution grid meet conformity. ABNT NBR IEC 62116 translates IEC 62116 and specifically addresses procedures for protection devices during grid interruptions, including equipment requirements and minimum standards an AIP must meet to be deemed functional. Internationally, standards such as IEEE 929:2000, IEEE 1547:2003, and IEC 62116:2014 are key. IEEE 929:2000 outlines guidelines on equipment and functions for the safe integration of photovoltaic systems with the grid, specifying inverter operation and testing conditions for AIPs. IEEE 1547 further specifies technical requirements for integrating distributed resources with the power distribution segment, including provisions for unintentional islanding protection and offering calculations for local load configuration during anti-islanding testing.

It is clear from these standards that unintentional islanding is a significant concern, as it can lead to operational risks and hazards for workers and users of the electrical system. The main risks associate to an unintentional islanding include electrical accidents, equipment damage from sudden frequency and voltage changes, and risks from out-of-phase reclosures. The main causes of unintentional islanding include maintenance procedures, electrical faults near the DGS, human error, or sabotage. While the abovementioned Standards establish the minimum AIP requirements, they do not specify a particular protection approach, leading

academic and industrial researchers to develop a diverse array of anti-islanding algorithms (TEODORESCU; LISERRE; RODRIGUEZ, 2011).

AIP schemes can be categorized by location and impact on power quality: remote methods are grid-side, while local methods are integrated into the inverter. Passive methods detect islanding by monitoring electrical changes after disconnection without disturbing the system, thus maintaining power quality. Active schemes, however, introduce disturbances in power factor, waveform, or frequency to detect islanding more aggressively. Key criteria for assessing AIP methods include power quality impact, detection time, Non-Detection Zone (NDZ), and multi-DG detection capability. Passive methods excel in power quality but may miss islanding in balanced loads, while selecting an optimal AIP requires testing across different conditions to understand each method's strengths and limitations.

It is also important to consider that although the active AIP demands power quality degradation, the evolution of the AIP literature produced a significant reduction of the harmonic distortion caused by the active solutions. Some methods use the concept of the positive feedback in order to guarantee more efficiency on islanding detection and, concomitantly, reduce power quality degradation. Other schemes use the concepts of bilateral or intermittent perturbation. The main goal of this text is to propose a new AIP scheme that will congregate the concepts of frequency drift, frequency positive feedback and intermittent bilateral perturbation that will accomplish faster detection and lower NDZ compared to other well-known AIP schemes. Beyond to propose a new anti-islanding technique, this text also goals to analyze some of the main AIP schemes according to three criteria: NDZ, detection time and THDi. The tests will be conducted for three different values of quality factor and in four environments: a single inverter-based DGS, double, triple, and quadruple inverter-based DGS. The analyzed methods will be: Active Frequency Drift (AFD), Sandia Frequency Shift (SFS), AFD by (CHEN et al., 2013), AFD with Pulsating Chopping Factor (AFDPCF) and Active Phase Jump with Positive Feedback (APJPF).

1.4 General Goals

This work covers the AIP addressed by the main Standards as a mandatory security issue for the interconection of renewable resources into the utility grid. Thus, the present text will conduct a complete review of the AIP literature, highlight the main remote, local passive and local active strategies, discussing its strengths and drawbacks and will also present a new anti-

islanding algorithm that will be able to perform the islanding detection for loads with quality factor in the range of $\mathbf{0 < Q_f \leq 5}$. It will also demonstrate the robustness of the strategy in detecting islanding in different multi-inverter configurations.

1.4.1 Specific Goals

Succinctly, the specific goals of the present work are:

- Provide a solid theoretical foundation for the comprehension of the islanding phenomenon, highlighting the main causes and effects and the influence of the local loads on electrical parameters after grid interruption;
- Conduct a survey analysis of the main schemes of remote, local passive and local active AIP, highlight the main strengths and drawbacks of each one. The survey will contemplate the main efforts of the AIP research to correct the main weakness of each solution;
- Present the main Standards recommendations about the AIP;
- Mapping the NDZ of each one of the analyzed AIP, including the proposed method;
- Perform a computational study for evaluate the performance of analyzed AIP methods according to three qualitative criteria: NDZ, THDi and detection time;
- Determine the capability of the proposed solution to work under a multi-DG based islanding occurrence;
- Perform the experimental evaluation of the proposed method using Typhoon ® Hil 404;
- Carry out an experimental comparison between the proposed method and other well-known anti-islanding strategy.
- Evaluate the performance of the proposed strategy in parallel with the other implemented solutions in a double and triple inverter;
- Present auxiliar concepts for the better understanding of the islanding phenomenon.

1.5 Methodology

The study begins by addressing foundational concepts essential for understanding islanding theory. Chapter two introduces Grid-Tie Photovoltaic Systems (GTPS), including topics like GTPS configurations, Maximum Power Point Tracking (MPPT), Phase Locked-Loop (PLL), and relevant Standards. The following chapter reviews the AIP literature, detailing

islanding theory, Non-Detection Zones (NDZ), various remote and local islanding detection methods, and the theoretical basis for the proposed AIP method. Chapter four focuses on the computational modeling of a GTPS with an RLC load as per AIP testing standards and a double-inverter DGS. Anti-islanding tests will be conducted across various quality factor and capacitance values, assessing NDZ, THDi, and detection time.

The next phase involves experimental testing of the new algorithm. Recognizing a lack of compatibility studies for recent AIP methods with existing solutions, this work includes real-time implementation of the proposed AIP alongside other AIP techniques to evaluate parallel performance. Finally, the last chapter will present comparative findings on the AIP strategies. In a summarized way, the main steps of this work are:

A. Literature review about the main topics of the islanding theory, considering the main causes and consequences of the phenomenon, the presentation of the NDZ problem and the main technologies for its mapping and a survey of the main remote, local passive and local active strategies applied to the islanding detection.
B. Proposal of a new AIP strategy able to detect the grid interruption for RLC loads with quality factors in the range of $0 < Q_f \leq 5$ in the single and in the double inverter-based DGS.
C. Computational analysis of the proposed anti-islanding scheme in comparison with other popular and well-known islanding strategies.
D. Review of the auxiliars concepts for the better understanding of the islanding phenomenon.
E. Practical realization of two inverters structures in order to develop a single inverter GTPS and a double inverter-based DGS.
F. Experimental evaluation of the proposed AIP algorithm and comparative study with other well-known AIP strategies in Typhoon ® Hil device.

1.6 Work Structure

In order to present the work in a organized way and clarify the reader understanding, the text is structured as following:

Chapter 2 – Grid-Tie Photovoltaics Systems

The Chapter 2 goals to present auxiliars concepts for the better understanding of the photovoltaics electrical power generation and, consequently, the islanding phenomenon. It will highlight the most common GTPS configurations, the Maximum Power Point Tracking algorithms, the sychronization techniques and the Standards related to the interconnection between the GTPS and the main utility grid.

Chapter 3 – Anti-Islanding Methods.

The Chapter 3 will show the theory of the islanding phenomenon theory, the Non-Detection Zone issue and the main technologies for its determination, the differences between the remote, local passive and local reactive AIP algorithms. Moreover, this chapter will also present the proposed scheme, with a detailed analysis of its NDZ and the new potentialites of the strategy.

Chapter 4 – Computational Results.

The Chapter 4 will present the computational realization of two DGS environments: a single inverter-based GTPS and a double inverter-based GTPS. Futhermore, it will be shown the results obtained by the implementation of the analyzed AIP algorithms under a proposed test methodoly. This methodology, by its time, will be based on the Standards considerations and will englobe the most restrictive recommendations. Finally, the results will be compared according to three key performance indicators: time detection, THDi and NDZ.

Chapter 5 – Real-Time Implementation Results.

The Chapter 5 will present the real time implementation of the proposed AIP using Typhoon ® Hil. It will also address the implementation of the other methods. Posteriorly, it will present results related to harmonic distortion of current before and after each strategy. Beyond that it will compare the performance of the AIP strategies in a single inverter based DG. It will also evaluate the performance of the APJPFIP working in parallel with the cited methods in a double, triple and quadruple inverter based DGS.

Chapter 6 – Conclusions and Discussions.

The final chapter will discuss the obtained results and compare them with the exposed theory.

1.7 Final Considerations

Recent advancements in electrical energy processing have enabled renewable energy-based Distributed Generation Systems (DGS) to integrate into the power grid, aiming to reduce global warming and, in Brazil, lessen dependence on hydroelectric power. However, increased DGS penetration poses challenges, notably unintentional islanding—where DGS continues operating after an unexpected grid disconnection, risking safety, power quality, and synchronization.

This study proposes a new Active Islanding Protection (AIP) algorithm that introduces a phase shift in the inverter's output current at each half-cycle, with positive frequency feedback to improve detection by tying frequency error to the disturbance. The method uses frequency alarm limits to speed up detection, reduce detection time, and minimize the Non-Detection Zone (NDZ) without excessive harmonic distortion. Effectiveness will be evaluated through simulations and real-time tests across varying conditions. Additionally, the study includes a comprehensive review of AIP literature, detailing the evolution of strategies and providing introductory material for understanding unintentional islanding.

CHAPTER II

Grid-Tie Photovoltaics Systems

2.1 Introduction

Grid-Tied Photovoltaic Systems (GTPS) consist of photovoltaic (PV) modules that convert solar energy into electrical energy, an inverter that interfaces the DC voltage and current levels with the electrical grid, and a filter that mitigates harmonic distortion in the inverter's output current.

During grid connected operation, the utility grid provides the references of voltage and frequency and the inverter imposes an active power flow from the panels to the local loads. If the power generated by the PV array is bigger than the power demanded by the loads, the surplus energy is exported to the grid. Otherwise, if the GTPS power is not able to match load demand, the grid provides the required extra power and guarantee the electrical feeding of all the devices connected to the PCC. There is also an exceptional but important contingency in which is verified a balance between solar generation and load consumption. In this scenario, the utility grid did not receive or transmit active power and, therefore, it is the most challenging condition for islanding detection.

This chapter will cover some of the main concepts of the connection of the GTPS into the main utility grid, highlighting the GTPS configurations, the Maximum Power Point Tracking (MPPT) algorithms, the Phase Locked-Loops (PLL) and the main Standards that addresses the AIP as a fundamental feature for commercial inverters.

2.2 GTPS Configurations

According to (ČORBA et al., 2012), GTPS configurations can be categorized into four types: central inverter, Multi String inverter, power optimizer and microinverter. Each one of this configurations has its vantages and advantages and, therefore, must be known by aplication engineerings and GTPS designers.

The central inverter configuration connects the entire solar array to a single inverter, which aligns the DC current and voltage levels with the grid. This setup is primarily beneficial due to lower installation costs. However, it suffers from reduced reliability, as a single fault in

the inverter can halt the entire system. Additionally, efficiency losses are noted because the MPPT algorithm is centralized.

In the multi-string configuration, several inverters divide the electrical output from the PV system, which raises installation costs but improves both reliability and efficiency by decentralizing MPPT control. Another notable configuration is the microinverter setup, where each photovoltaic module has an individual inverter. While more expensive, this arrangement enhances both reliability and efficiency, particularly in installations that experience shading (Hernandez-Vidal et al., 2017).

2.3 Maximum Power Point Tracking (MPPT)

Photovoltaic systems have a Maximum Power Point (MPP), a specific voltage and current pair (V;I) that maximizes power extraction from the PV array. An MPPT algorithm is any method or device that aims to find this optimal operating point, essential for maximizing installation efficiency and optimizing payback time (ISHAQUE; SALAM, 2013).

The MPP is dynamic and varies with conditions like temperature, irradiance, and partial shading—where sections of a solar module receive less sunlight, distorting the power-voltage (P-V) curve and creating multiple local MPPs. (MOHAPATRA et al., 2017) offers a review of MPPT algorithms, especially those capable of determining MPP under partial shading conditions.

2.4 Phase Locked Loop (PLL)

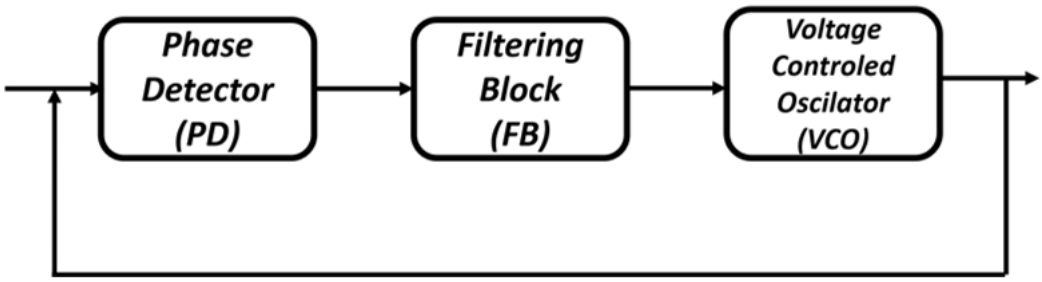
The successful integration of the DGS depends on the obedience to the quality criteria defined by the Standards (IEEE, 2000) (ANBT, 2013). Once the inverter must work in parallel with the main utility grid, the GTPS output current must be in synchronism with the main grid, this is, must have the same phase and frequency characteristics than the PCC voltage. To address this, the literature has proposed different synchronization strategies, being possible to divide them in two groups: open-loop methods and closed-loop methods.

The Open Loop Synchronization can be based on zero crossing detection or in the filtering of the grid voltage. The ZCD strategy has the advantage of implementation simplicity, either digitally or analogically. However, this kind of solutions loses efficiency in high polluted grid conditions and lacks accuracy under instrumentation noises. The synchronization based on the

filtering of the input voltage, by its time, presents difficulties to follow the natural phase and frequency oscillations of the electrical system dynamics. Therefore, the state of the art of the inverter synchronization are the Phase-Locked Loop (PLL) techniques.

A PLL is a closed-loop control system that takes a periodic input signal and generates a synthetic one with identical phase and frequency characteristics. This approach enables robust synchronization, even in distorted grid conditions, and it effectively tracks grid phase and frequency variations. PLLs can also extract real-time phase and frequency information, which improves islanding detection performance. Figure 2.1 outlines the basic structure of a PLL, showing the Phase Detector (PD), Filtering Block (FB), and Voltage Controlled Oscillator (VCO).

Figure 2.1 – Generic Representation of a PLL



Source: Author.

The Phase Detector (PD) plays a crucial role by comparing the input voltage with the generated output to determine any phase error between the two signals. This comparison can be performed through various methods, such as using multipliers, the Park Transform, or adaptive filtering. Once the PD identifies the phase error, the Filtering Block (FB) works to reduce it. This mitigation process can employ either a low-pass filter, a proportional-integral controller, or a combination of both to ensure accurate error correction. Finally, the Voltage-Controlled Oscillator (VCO) generates an output signal that mirrors the input voltage's phase and frequency, while also calculating these parameters to maintain synchronization (SOUZA et al., 2019).

2.4.2 PLL SOGI

Proposed in (CIOBOTARU; TEODORESCU; BLAABJERG, 2006), this PLL approach is based on the adoption of an adaptative filter with a second order integrator to perform the phase detection, as illustrated by Figure 2.2. The equation (2.1) demonstrates the transfer

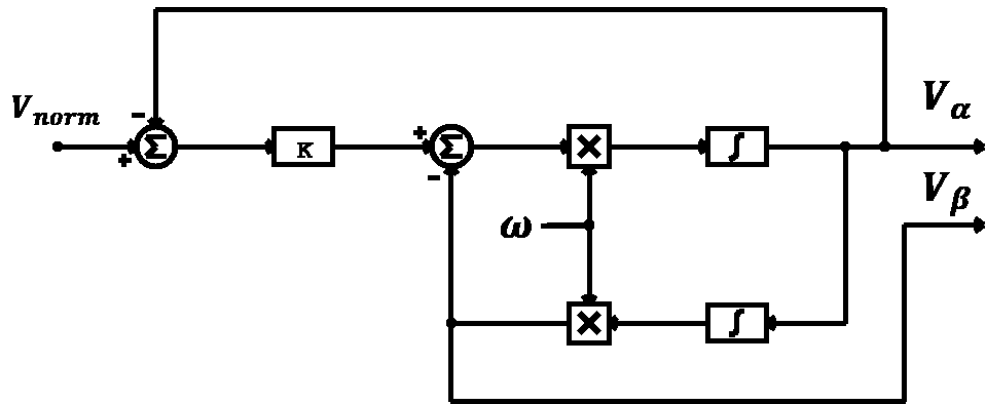
function of the Second Order Generalized Integrator (SOGI) filter, while (2.2) and (2.3) represent the closed loop transfer function relating the input to each one of the two outputs $H_\alpha(s)$ and $H_\beta(\mathrm{s})$, respectively. Finally, the Figure 2.3 demonstrates the complete SOGI PLL diagram.

$$H(s) = \frac{s\omega}{s^2 + \omega^2} \tag{2.1}$$

$$H_\alpha(s) = \frac{k_{sogi} s\omega}{s^2 + ks\omega + \omega^2} \tag{2.2}$$

$$H_\beta(s) = \frac{k_{sogi}\omega}{s^2 + k_{sogi} s\omega + \omega^2} \tag{2.3}$$

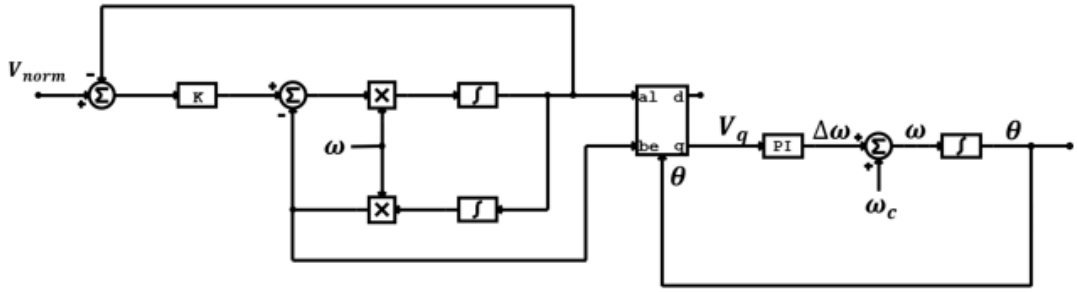
Figure 2.2 – SOGI filter block diagram.



Source: (SOUZA et al., 2019).

In (SOUZA et al., 2019), a computational comparison was performed on three distinct PLL algorithms: the Classic PLL, a time-delay-based PLL (GAUTAM et al., 2019), and the SOGI PLL. This analysis evaluated performance across frequency, phase, and amplitude variations, with findings indicating that the SOGI PLL achieved the shortest settling time and superior performance regarding frequency stability and phase accuracy. These results influenced the choice of the SOGI PLL for synchronizing the inverter with the utility grid in the AIP tests for the current study. Additionally, the SOGI PLL can be adapted for active islanding detection(CIOBOTARU; AGELIDIS; TEODORESCU, 2008).

Figure 2.3 – SOGI PLL block diagram.



Source: (SOUZA et al., 2019).

2.5 Standard Considerations

The GTPS effective integration into the power grid requires compliance with operational and safety standards. These standards, developed by various national and international organizations, define limits for total harmonic distortion (THD) during normal operation, allowable ranges for voltage and frequency fluctuations, maximum DC levels permissible in inverter output current, power factor stability thresholds, and minimum inverter protection requirements. Additionally, they all agree on the necessity of Active Islanding Protection (AIP). Table 2.1 lists the main regulatory documents referenced in this study..

Table 2.1 – Grid Tie Photovoltaics Standards.

Standards	***Description***
ABNT NBR 16149	Photovoltaics (PV) systems – Characteristics of the utility interface
IEEE 1547	IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems
IEEE 929	IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems
ABNT NBR 62116 IEC 62116	Test procedure of islanding prevention measure for utility-interconnected photovoltaic inverters.

Source: Author.

2.5.1 Voltage Variation Thresholds.

Voltage disturbances and fluctuations at the Point of Common Coupling (PCC) may arise temporarily due to load disturbances or persistently due to faults in the electrical system.

Therefore, a maximum allowable duration for such abnormalities has been established to prevent unnecessary operational interruptions. Table 2.2 outlines the maximum operation times for a Photovoltaic System (PV) under various voltage fluctuation magnitudes..

Table 2.2– Grid-Tie Photovoltaics Standards: Voltage operational thresholds.

IEEE 929-2000		**IEEE 1547-2003**		**ABNT 16149**	
Range (%)	Time (s)	Range (%)	Time (s)	Range (%)	Time (s)
V<50	0.1	V<50	0.16	-	-
50≤V≤88	2	50≤V<88	2	V<80	0.4
88≤V≤110	∞	88≤V≤110	∞	80≤V≤110	∞
110≤V≤137	2	110≤V<120	1	110<V	0.2
137≤V	0.1	V≥120	0.16	-	-

Source: Adapted from (IEEE, 2000), (IEEE, 2003), (ABNT, 2013)

2.5.2 Frequency Variation Thresholds.

Inverters connecting a DGS to the main grid must ensure that the current they supply aligns in frequency and phase with the grid voltage. However, minor fluctuations in grid frequency may occur due to typical electrical events, such as motor switching, the disconnection of nearby generation systems, or sudden changes in local load impedance near the PCC. To account for these variations, standards specify upper and lower frequency limits within which the inverter can function, along with corresponding time intervals required for proper inverter shutdown, as outlined in Table 2.3.

Table 2.3– Grid Tie Photovoltaics Standards: Frequency operational thresholds.

IEEE 929-2000		IEEE 1547-2003		ABNT 16149	
Range (Hz)	Time (s)	Range (Hz)	Time (s)	Range (Hz)	Time (s)
f<59,5	0.1	f<59.3	0.16	f<58.5	0.2
f>60,5	0.1	f>60.5	0.16	f>61,.5	0.2

Source: Adapted from (IEEE, 2000), (IEEE, 2003), (ABNT, 2013)

2.5.3 Harmonic Distortion of Current.

In inverter based DGS maintaining power quality becomes increasingly challenging, since inverters devices operate on semiconductor switching principles, which can lead to higher harmonic content. To reduce the impact of DGS on power quality, standards recommend maximum allowable levels for both total and individual harmonic content that an inverter can

produce at its nominal operating point. These recommended thresholds are outlined in Table 2.4.

Table 2.4 – Grid Tie Photovoltaics Standards: Harmonic distortion of current.

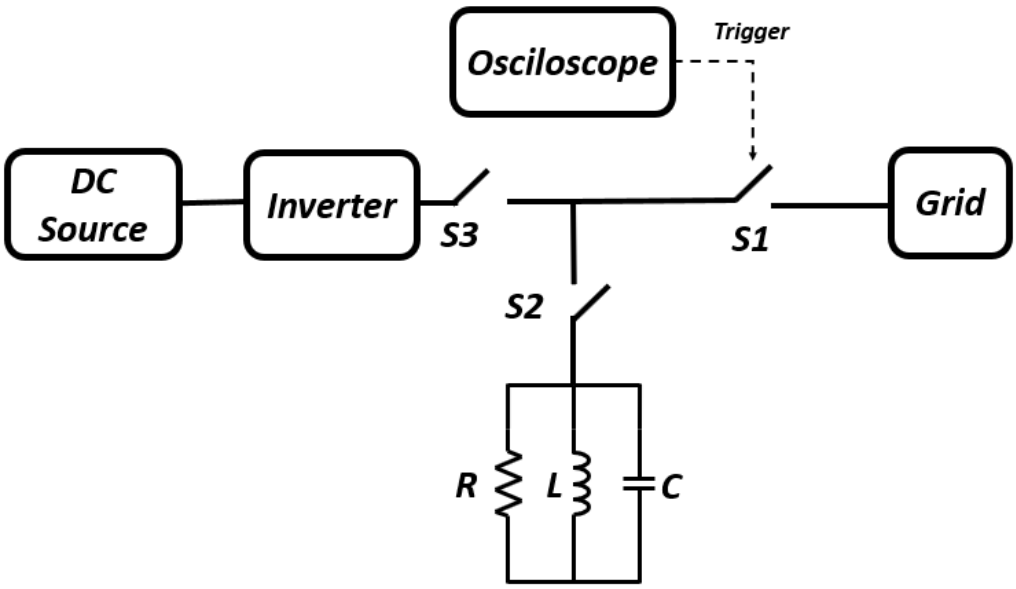
IEEE 929-2000		IEEE 1547-2003		ABNT 16149	
Order (h)	Limit	Order (h)	Limit	Order (h)	Limit
3-9	< 4.0 %	3-9	< 4.0%	3-9	< 4.0%
11-15	< 2.0 %	11-15	< 2.0%	11-15	< 2.0%
17-21	< 1.5%	17-21	< 1.5%	17-21	< 1.5%
23-33	< 0.6 %	23-33	< 0.6%	23-33	< 0.6%
Pair orders must be below of 25% of the even orders limit.				2-8	< 1.0 %
				10-32	< 0.5 %
Total	< 5.0 %	Total	< 5.0 %	Total	< 5.0 %

Source: (IEEE, 2000), (IEEE, 2003), (ABNT, 2013)

2.5.4 Anti-Islanding Protection

Figure 2.4 shows the basic setup for AIP testing, which includes a DC source, an RLC parallel load, and an AC source that can be replaced by the electrical grid if certain criteria are met (to be discussed in later sections). Anti-islanding protection is essential for inverter commercialization and DGS grid connection, national and international standards outline minimum requirements for AIP performance. While there is no specification on whether AIP should be a physical device or embedded software, nor on active versus passive methods, all standards agree on the same configuration for islanding detection testing.

Figure 2.4 – Anti-Islanding test recommended set up.



Source: (IEEE, 2000), (IEEE, 2003), (ABNT, 2013)

2.5.4.1 AIP Recommendations: IEEE 929-2000

The first testing condition involves verifying inverter operation while connected to the power grid. According to the guidelines, anti-islanding testing can be conducted either with an AC source or by connecting to the utility grid. Recommendations for this process specify that voltage must be controlled within 2% of its strictest limits, and frequency may vary by up to ±0.1 Hz.

The next step is determining the RLC load to be used for testing. This can be done with switch S2 closed, allowing power flow from the grid to the load. The resistor should consume the full power output from the simulated Distributed Generation (DG) system. Additionally, the standard specifies that the LC pair's quality factor must remain at 2.5. Given that the quality factor is the ratio of reactive power to active power, for an active power level P_{load}, the reactive demand should be:

$$Q_{load} = 2.5.P_{load} \tag{2.4}$$

The first parameter to be considered is the inductive one, that must be adjusted until the relation (2.5) be satisfied.

$$Q_{inductor} = Q_{load} \tag{2.5}$$

Posteriorly, must be conducted the insertion of the capacitive parameter must adhere the relation (2.6).

$$Q_{capacitor} = Q_{inductor} = Q_{load} \tag{2.6}$$

The resistive component is connected in parallel with the LC pair, with switch S1 connecting the main grid to the PCC, S2 linking the grid to the equivalent load, and S3 allowing power flow between the inverter and the load. Given non-ideal load characteristics, instrumentation inaccuracies, and PCC voltage harmonics, experimental adjustments to load parameters are necessary to minimize current from the grid to the load.

Beyond nominal testing, it’s recommended to test the AIP across varying load levels and inverter output powers, as detailed in Table 2.5. Additionally, ±1% adjustments should be made to the resistive and capacitive parameters, covering the range from 95% to 105%. Across all scenarios, islanding detection must occur within 2 seconds.

Table 2.5– (IEEE, 2000) power levels recommendations for the AIP test.

Tests Conditions	Load Power	Inverter Power
1	25%	25%
2	50%	50%
3	100%	100%
4	125%	100%

Source: (IEEE, 2000).

2.5.4.2 AIP Recommendations: IEEE 1547-2013

The (IEEE, 2013) determines the same setup for islanding detection testing. However it stablishes the equations for load parametrization to reach the above-mentioned recommendations. The equations (2.7), (2.8) and (2.9) demonstrate the calculus of R, L and C, respectively.

$$R = \frac{V^2}{P} \tag{2.7}$$

$$L = \frac{V^2}{2\pi f_0 P Q_f} \tag{2.8}$$

$$C = \frac{Q_f P}{2\pi f_0 V^2} \tag{2.9}$$

Tests should be repeated by adjusting one of the reactive load parameters (either the inductor or capacitor) up or down by 1%, to reach 95% and 105% of its nominal value. If PAI response times increase at 95% or 105%, further 1% adjustments should be made until response times decrease. This sequence of tests must also be conducted at 66% and 33% of the inverter's capacity. If the inverter cannot operate at 33%, the lowest operable power level should be used. The maximum allowed response time is 2 seconds (IEEE, 2003).

2.5.4.3 AIP Recommendations: ABNT NBR 62116

The purpose of (ABNT, 2012) is to establish a test methodology for anti-islanding algorithms or devices specifically designed for single or three-phase SGD systems, taking into account their distinct characteristics. This Standard is a direct translation of (IEC, 2008) and focuses exclusively on islanding detection, distinguishing it from earlier standards like (IEEE, 2000) and (IEEE, 2003), which address all aspects of renewable energy resource interconnection with the distribution grid.

It defines that the fundamental current component from the grid to the PCC should be under 1% of the inverter's fundamental output power component. Anti-islanding tests must be performed at 100%, 66%, and 33% of the inverter's rated output power, as shown in Table 2.6. If the inverter cannot operate at 33% of its rated power, testing should proceed at the lowest operable fraction of output power.

Table 2.6– (ABNT, 2012) power levels recommendations for the AIP test.

Contidion	***Power***
A	Rated
B	50%-66% of the Nominal Power
C	25%-33% of the Nominal Power

Source: (ABNT, 2012)

For condition A, the load parameters must be adjusted according the Table 2.7. Each cell is composed by an ordered pair. The first value of the ordered pair is the percentual variation that must be imposed to the resistive parameter and the second valor represents the percentual variation of the reactive parameter (capacitance or inductance). The cells filled in red are the mandatory tests. The detection time for those conditions must be compared with the detection time for the central condition (0%;0%) and, if one of them is bigger than the detection time for the nominal point, all of the other test of the table must be performed.

Table 2.7 – AIP tests for condition A

-10 %, 10 %	-5 %, 10 %	0 %, 10 %	5 %, 10 %	10 %, 10 %
-10 %, 5 %	-5 %, 5 %	0 %, 5 %	5 %, 5 %	10 %, 5 %
-10 %, 0 %	-5 %, 0 %	0 %, 0 %	5 %, 0 %	10 %, 0 %
-10 %, -5 %	-5 %, -5 %	0 %, -5 %	5 %, -5 %	10 %, -5 %
-10 %, -10 %	-5 %, -10 %	0 %, -10 %	5 %, -10 %	10 %, -10 %

Source: (ABNT, 2012)

For test conditions B and C, similar procedures to those outlined in the referenced Standards should be applied. This involves adjusting the resistive parameter and one of the reactive parameters in ±1% increments to cover all values from 95% to 105%. If the detection time under boundary conditions exceeds the detection time observed during testing with nominal load parameters, additional ±1% increments should continue until a reduction in detection time is observed. Table 2.7 presents the detection times for various islanding scenarios.

Table 2.8 – (ABNT, 2012) frequency and voltage thresholds.

Parameter	*Magnitude*	*Time (s)*
Under voltage	85%	2
Over voltage	115%	2
Under frequency	58.5 Hz	1
Over frequency	61.5 Hz	1

Source: (ABNT, 2012)

2.6 Final Considerations

Effective renewable energy integration relies on meeting minimum safety and quality standards, which specify essential parameters for GTPS devices and algorithms to ensure DGS reliability and operator safety. This chapter reviewed main GTPS configurations, including MPPT techniques, highlighting the importance of choosing a robust PLL strategy for AIP, particularly the SOGI PLL, known for minimizing frequency estimation oscillations. Additionally, it covered major standards for DGS grid integration, such as (IEEE, 2000), (IEEE, 2003), and (ABNT, 2013), addressing voltage and frequency stability, THDi limits, and islanding detection requirements. The next chapter will delve into various AIP methods, dividing them into passive and active approaches.

CHAPTER III

3. Anti-Islanding Methods

3.1 Introduction

The anti-islanding solutions can be divided according to their principle of operation or location. In relation to the location, the methods resident at the grid side can be called of remote and the techniques based on the inverter side are called of local methods.

As a result, the remote solutions are more reliable and freer of NDZ. However, the price and complexity of implementation are serious drawbacks to its adoption for small or medium DGS. The main representative of this class of AIP can be categorized in: impedance insertion, power line carrier communication and transfer trip schemes.

The local strategies, on the other hand, are known by its non-cost implementation and can be easily embedded in the inverter microprocessor, being divided in passive or actives. The passive techniques are defined by the pure monitoring of a PCC variable such as: under/over voltage (OUV) or frequency (OUF), Phase Jump (PJ) detection, Harmonic Distortion (HD) detection, Rate of Change of Frequency (ROCOF), Voltage (ROCOV), Phase Angle Difference (ROCPAD), Active Power (ROCOP) or Reactive Power (ROCORP). Nevertheless, the passive AIP is marked by considerable NDZ issues, being unable of detecting the grid interruption in power balance conditions. In this context, the active solutions emerged. These methods are defined by the insertion of small perturbations into the PCC to deviate the inverter operation to out of the range of the Standards allowed values.

Summarizing, this chapter is destinated to explain the principle of operation of the mains representative AIP. Beyond this, it will explain the concept of NDZ and its mapping methodologies.

It is important to highlight that the main information has been reported in Ê. C. Resende, M. G. Simões and L. C. G. Freitas, "Anti-Islanding Techniques for Integration of Inverter-Based Distributed Energy Resources to the Electric Power System," in IEEE Access, vol. 12, pp. 17195-17230, 2024, doi: 10.1109/ACCESS.2024.3357710. The AIP literature survey presented in this chapter is an essential part of the research and brings original contributions and, therefore, is part of this work.

3.2 Non-Detection Zone (NDZ)

The Non-Detection Zone (NDZ) refers to the range of load conditions in which an AIP is unable to detect a grid disconnection. It is a crucial qualitative measure for assessing the performance of an AIP scheme, particularly for frequency drift-based methods. The literature has identified four main methodologies for mapping the NDZ: the ΔP x ΔQ plan, the $L\ x\ C_{norm}$ plan, the $Q_f\ x\ f_0$ plan and the $Q_f\ x\ C_{norm}$ plan.

The ΔP x ΔQ plot stablishes the active and the reactive power flow from grid to load in the imminence of the islanding. This map is indicated to passive strategies since its losses efficiency when it comes to active strategies (SILVA, 2016). For guarantying the mapping of active methods NDZ, (ROPP et al., 2000a) proposed the $L\ x\ C_{norm}$ which links load inductance with normalized capacitance, defined by Equation 3.1. While this plot is suitable for active AIP schemes, it does not account for resistive load parameters (R), requiring a separate NDZ mapping for each R value (YU; MATSUI; YU, 2010).

$$C_{norm} = \frac{C}{\omega_o L} \tag{3.1}$$

Where:

- C – Load Capacitance [F];
- ω_o – Nominal grid angular frequency [rad/s];
- L – Local Load Inductance [H];

As NDZ mapping evolved, (LOPES; SUN, 2006) proposed the $Q_f\ x\ f_0$ plot, which relates the load quality factor Q_f to its resonance frequency (f_0). Q_f, defined as the ratio of power absorbed to power consumed by the load, is given by Equation 3.2. The resonance frequency is the frequency at which inductive and capacitive reactance are equal. This method is advantageous because quality factor is a function of load resistance (R), eliminating the need to plot the NDZ for each R value (RESENDE; SIMÕES; FREITAS, 2024).

$$Q_f = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{3.2}$$

Where:

- C – Load Capacitance [F];
- R – Load Resistance [Ω];

Nonetheless, this plot methodology has a drawback in that it does not fully align with the recommendations of Anti-Islanding Standards, which require testing AIP schemes under various load reactive conditions. Therefore, (LIU; KANG; DUAN, 2007) proposed the $Q_f \; x \; C_{norm}$ plan that relates the load quality factor to the normalized capacitance. The NDZ is the region of the plane between a upper and a lower curve, as defined by Equation 3.3.

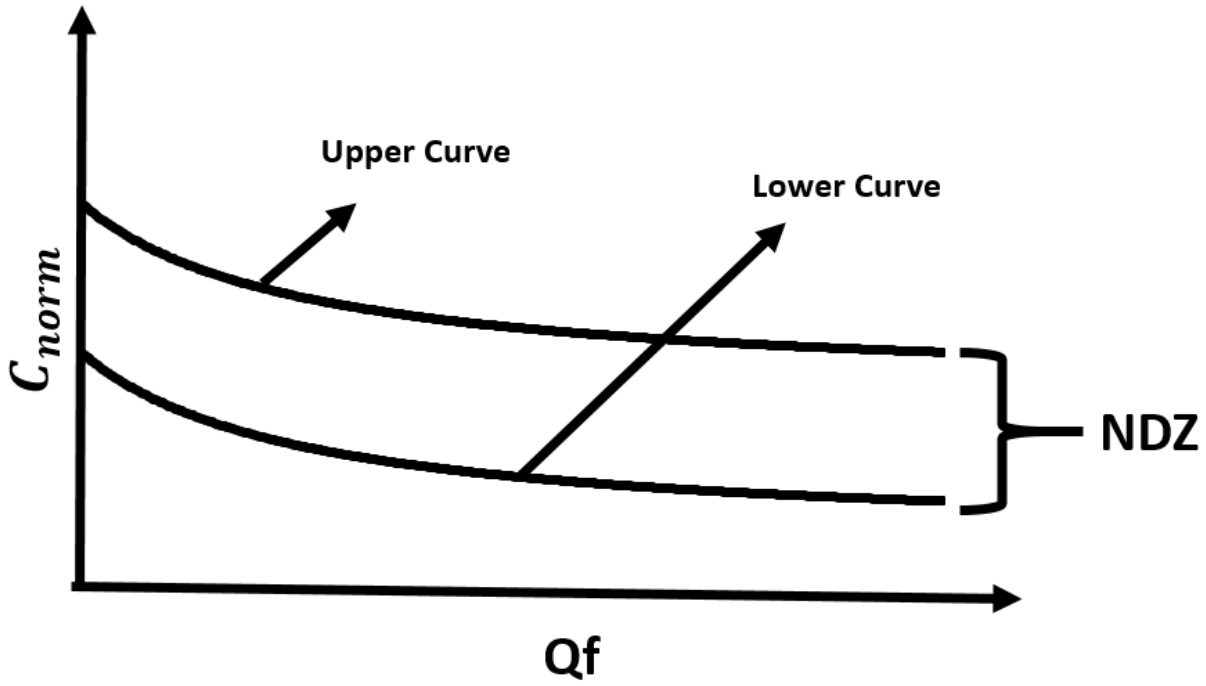
$$1 - \frac{2(\omega_{max})}{\omega_o} + \frac{tg(\theta_{inv})}{Q_f} < C_{norm} < 1 + \frac{2(\omega_{min})}{\omega_o} + \frac{tg(\theta_{inv})}{Q_f} \tag{3.3}$$

Where:

- $\omega_{min}, \omega_{max}$ – Minimum and maximum angular frequency thresholds, respectively.
- θ_{inv} – Phase difference between the PCC voltage and the inverter output current.

Finnaly, Figure 3.1 illustrates the upper and lower curve of a generic NDZ.

Figure 3.1 – Generic representation of a NDZ in the $Q_f x \; C_{norm}$ space.



Source: Author.

3.3 Remote Techniques

Remote or grid-resident AIP strategies rely on communication or signal processing technologies for islanding detection. These remote methods are advantageous as they avoid

several issues related to local AIP, such as reduced effectiveness in multi-DG islanding scenarios, impacts on power quality, and the presence of NDZ. However, remote detection methods are costly and complex to implement, making them economically unfeasible for small or medium DGS systems. The most common remote strategies include Power Line Carrier Communication (PLCC), Direct Transfer Trip (DTT), and External Capacitor Switching (ECS) (ETXEGARAI; EGUÍA; ZAMORA, 2011).

3.3.1 Impedance Insertion

The Impedance Insertion method involves the periodical switching an impedance, typically a capacitor bank, in order to deviate frequency after an unintentional grid interruption. The key drawbacks of this approach are high cost implementation, slow islanding detection, and large NDZ (Takigawa, Okamoto, Kobayashi, 1993). This method was extensively applied in early AIP studies at the Rokko Test Center in the 1990s (Kobayashi, Takigawa, Hashimoto, 1991; Takigawa, Okamoto, Kobayashi, 1993). However, the need for additional devices at the PCC and the associated high costs make it less appealing for widespread use.

3.3.2 Direct Transfer Trip

In Direct Transfer Trip (DTT) based anti-islanding strategies, all breakers capable of provocating the islanding of a DGS are monitored by a central master system that detects grid desconnection and identifies the affected areas (KIM et al., 2019). The performance of DTT relies on communication infrastructure, such as leased phone lines, radio, or dedicated fiber, and also requires a supervisory system. Like other remote AIP techniques, DTT offers high effectiveness and accuracy but faces challenges related to high costs and complex implementation, making it generally suited for high-power applications (WALLING, 2011).

In (LI; SAVULAK; REINMULLER, 2014), a study examined three islanding events at a power plant with hydraulic, natural gas, and wind-based generators using the DTT scheme for islanding protection. The data suggests that DTT should be avoided in systems with load-shedding capabilities to prevent long detection times. Additionally, it lacks performance if there are reactive compensators connected to the electrical islanding.

3.3.3 Power Line Carrier Communication

A Power Line Carrier Communication (PLCC) system consists of a transmitter (T) on the utility grid side and a receiver (R) that exchanges information via the power line instead of

using telecommunication tecnology. Typically, the islanding signal is transmitted over four conduction cycles, and the grid interruption is diagnosed if the signal disappears during this period (POLUEKTOV et al., 2016). For PLCC-based AIP schemes with communication lines longer than 15 km, repeaters are required (ETXEGARAI; EGUÍA; ZAMORA, 2011). Due to the high complexity and cost, there are few publications on this method.

The initial application of PLCC for islanding detection is presented in (ROPP et al., 2000b), emphasizing the crucial choice of transmission signal. This research shows that high-frequency signals are generally attenuated by distribution transformers' series inductors and should be avoided, particularly in small-scale generation systems. It also underscores that transmission speed should be minimized to simplify the system. The study used an existing automatic metering system alongside a low-cost custom receiver to keep costs down and established guidelines for making PLCC-based AIP solutions economically viable.

In (BENATO; CALDON; CESENA, 2003), the performance of a PLCC-based AIP was evaluated in a real megawatt-scale dispersed generation setup, analyzing how natural line factors like length, cable type, and load characteristics influence signal attenuation. Research by (CATALIOTTI et al., 2012) explored signal attenuation in medium-voltage transformers, deriving a mathematical model for this effect. Lastly, a sensitivity analysis for a PLCC AIP system was conducted in (POLUEKTOV et al., 2017).

3.4 Local Passive Methods

Passive Islanding Detection (PID) refers to all AIP methods or devices that operate without introducing any disturbance into the inverter's functionality. Notably, Standards governing the integration of distributed generation (DG) with the grid mandate several protections against voltage and frequency deviations, short circuits, and similar contingencies. Therefore, islanding detection can leverage one of these required inverter protections, avoiding any additional computational demands. However, PID presents ploblems related to low efficiency and considerable NDZ. This work will explore several PID approaches, including Over/Under Voltage (OUV/OUF), Phase Jump (PJ) detection, Harmonic Distortion (HD) detection, Rate of Change of Frequency (ROCOF), Rate of Change of Voltage (ROCOV), Rate of Change of Phase Angle Difference (ROCPAD), Rate of Change of Active Power (ROCOP), and Rate of Change of Reactive Power (ROCORP) (CEBOLLERO et al., 2022).

3.4.1 Over/Under Voltage (OUV) and Frequency (OUF)

The OUV/OUF methods involve monitoring and comparing values of voltage magnitude and frequency against standard thresholds. If any abnormalities are detected within a specified time frame, islanding is confirmed. This is one of the simplest AIP schemes since these features are inherently included in commercial inverters. The IEEE Standard (IEEE, 2008), "IEEE Standard for Electrical Power System Device Function Numbers, Acronyms, and Contact Designations," assigns specific codes to protection, monitoring, and control devices. The frequency monitoring device is designated with the ANSI code 81, while overvoltage and undervoltage protection are designated with ANSI codes 59 and 27, respectively.

According to (TEODORESCU; LISERRE; RODRÍGUEZ, 2011), after the grid interruption, the value of the PCC voltage will be controlled by the relation of the active power produced by the inverter and the active power demanded by the load as exemplified by (3.4). And the value of the frequency, after islanding formation, by (3.5).

$$V' = V\sqrt{\frac{P_{DGS}}{P_{load}}} \tag{3.4}$$

$$\omega' = \frac{-\frac{Q_{load}}{CV'} + \sqrt{\left(\frac{Q_{load}}{CV'}\right)^2 + \frac{4}{LC}}}{2} \tag{3.5}$$

Where:

- P_{DGS} – Active power produced by the DGS;
- P_{load} – Active power demanded by the local loads;
- Q_{load} – Reactive power consumed by the load;
- V – PCC voltage before the islanding;
- V' – PCC voltage after the islanding;
- ω' - DGS angular frequency after the islanding;

As can be seen , $P_{DGS} = P_{load}$ implies on $V' = V$. Beyond that, if the RLC load is resonating at the grid nominal frequency, $Q_{load} = 0$ and (3.5) can be rewritten as (3.6), that is the exactly the expression of the resonance frequency. This way, it is easy to understand that, if the islanded load has the same or similar parameter values as described by the Standards AIP test recommendations, this method is simply unable to shut the inverter down after the grid interruption (BRITO et al., 2018).

$$\omega' = \frac{1}{\sqrt{LC}} \tag{3.6}$$

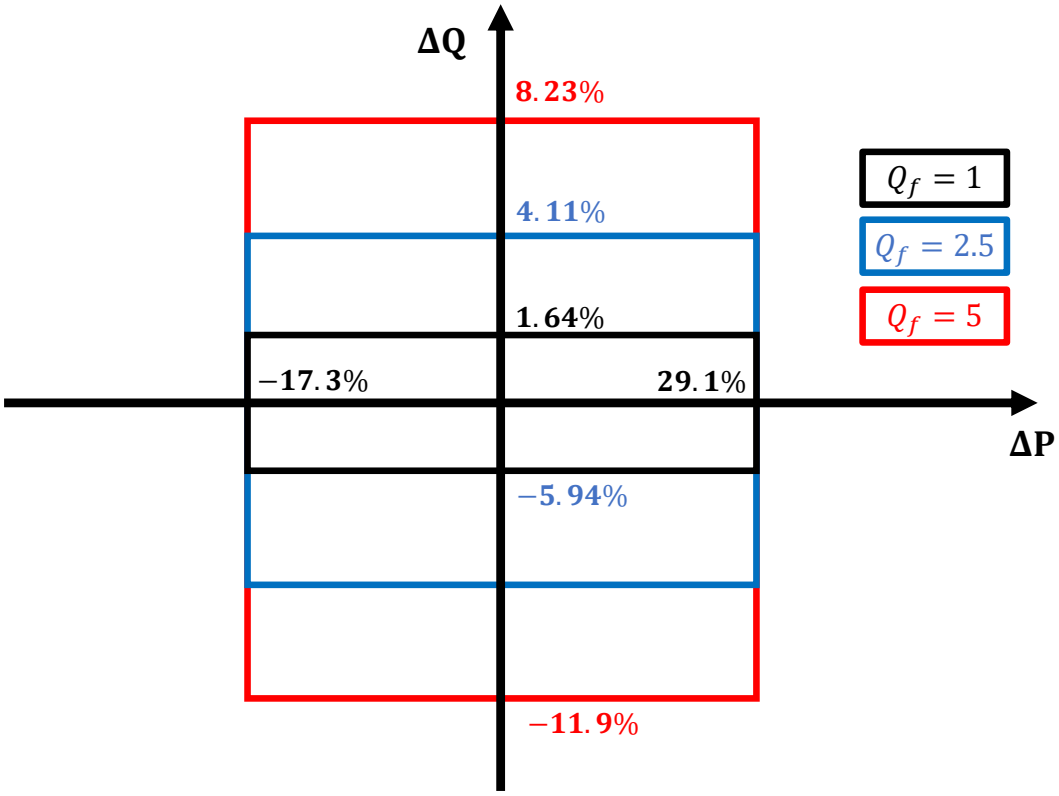
Mathematically, the NDZ of this method can be plotted in the ΔP x ΔQ plan through equations (3.7) and (3.8)

$$\left(\frac{V}{V_{max}}\right)^2 - 1 \geq \frac{\Delta P}{P} \geq \left(\frac{V}{V_{min}}\right)^2 - 1 \tag{3.7}$$

$$Q_f\left(1 - \left(\frac{f}{f_{min}}\right)^2\right) \geq \frac{\Delta Q}{P_{GD}} \geq Q_f\left(1 - \left(\frac{f}{f_{max}}\right)^2\right) \tag{3.8}$$

The graphical representation of this region is shown by Figure 3.2, considering the maximum and minimum frequency thresholds from (IEEE, 2003) and different values of quality factor. The ΔP axis is referent to the voltage variation and the ΔQ axis to the frequency variation. As can be seen , the voltage variation is not impacted by the variation of the quality factor. The frequency variation, on the other hand, is highly sensitive to the Q_f value.

Figure 3.2 – OUV/OUF NDZ plotted in the ΔP x ΔQ plan



Source: Adapted from (TEODORESCU; LISERRE; RODRÍGUEZ, 2011)

3.4.2 Phase Jump Detection (PJD)

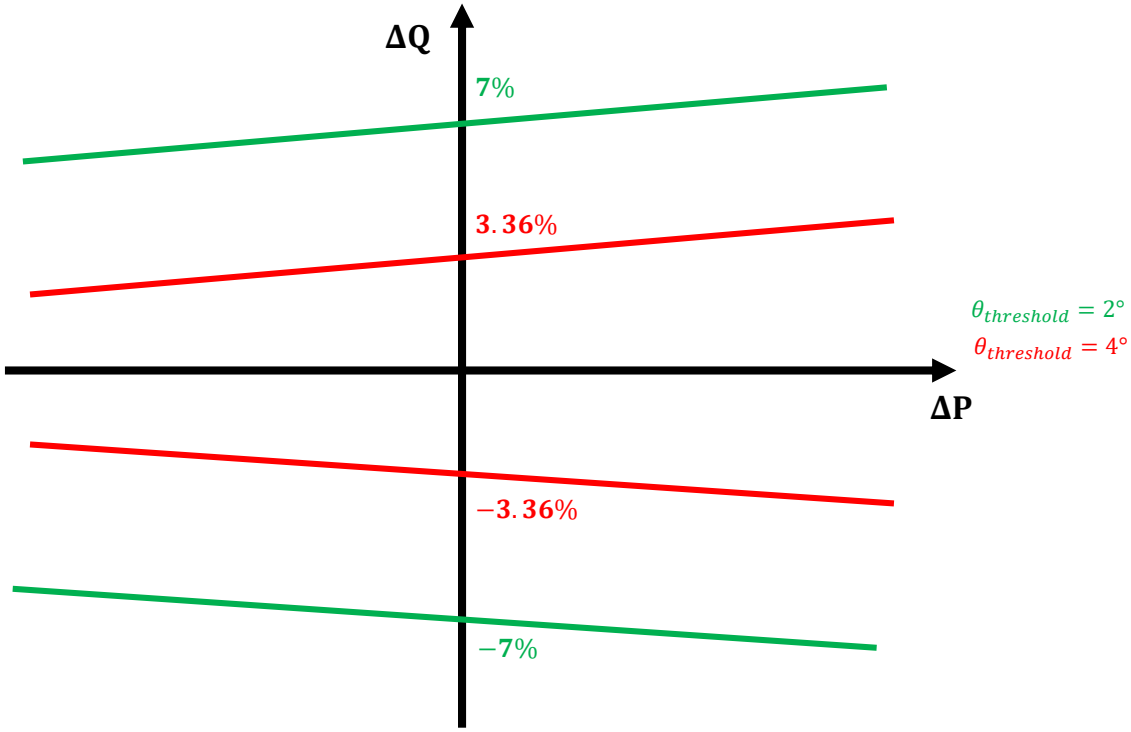
The PJD strategy monitors the angle difference θ_{inv} between the PCC voltage and the inverter output current. If is verified an abrupt change the islanding is confirmed and the protection system shuts the inverter down.

This strategy can present lower detection time compared to the OUV/OUF approach, because the phase dynamics is quicker than the frequency one (SINGAM; HUI, 2006). However, it is important to state that the some modern synchronization techniques, especially the modern Phase-Locked Loop (PLL) are capable of absorving the phase jump, leading to a false negative diagnosis. Its implementation is marked by the difficult of choosing a correct threshold to diagnosis islanding because there is no Standard recommendation about the phase jump (DE MANGO et al., 2007). Therefore, the design of the PJD algorithm depends on solid knowledge about the electrical system in which the inverter is installed. In addition, the PJD can cause nuisance trips after some non-islanding contigences as the starting of motors and the switching of a capacitor bank. (ABOKHALIL; AWAN; AL-QAWASMI, 2018).

Finally, the NDZ of the PJD algorithim is mathematically described by (3.9). As can be seen , the NDZ is not affected by the quality factor of the local load, what is an advantage compared to the previous PID scheme. However, it is dependent of the power generated by the load and of the chosen threshold. Figure 3.3 illustrates the NDZ for the PJD across various angle detection threshold values. Unlike the OUFV scheme, the PJD method exhibits undetectable cases across all values of ΔP.

$$abs\left(arctg\left(\frac{\frac{\Delta Q}{P}}{\frac{1+\Delta P}{P}}\right)\right) \leq \Theta_{threshold} \tag{3.9}$$

Figure 3.3 – PJD NDZ plotted in the ΔP x ΔQ plan for different values of $\boldsymbol{\Theta_{threshold}}$



Source: Adapted from (CEBOLLERO et al., 2022)

3.4.3 Harmonic Detection (HD)

This method monitors the harmonic content of the PCC voltage. During grid-connected mode, the THDv is caused by the relation between the current harmonic orders of the output current and the grid impedance. After the islanding event, nevertheless, the harmonic content of the PCC voltage is determined by the product between the current harmonic components and the load impedance that are generally bigger than the grid one (ABOKHALIL; AWAN; AL-QAWASMI, 2018).

Differently of the previous passive AIP methods, HD detection capabilities are not influenced by the relation between power generated and consumed (TEODORESCU; LISERRE; RODRÍGUEZ, 2011). However, the correct parameterization of a HD relay can be challenging. A small islanding threshold can result in false tripping of the inverter, while a larger threshold can increase the NDZ. Additionally, the algorithm lacks selectiveness, as various non-islanding events can cause an increase in THDv. Moreover, the algorithm can present lack of selectiveness due to non-islanding events (ALJANKAWEY et al., 2010). Non-linear loads (YOSHIDA; SUZUKI, 2014) and the grid background distortion (ELGENDY et

al., 2015) also impact its performance and the diagnosis threshold must be chosen based on previous knowledge of the system in which the inverter operates. Furthermore, the capacitance of local loads can filter out high-frequency harmonic components, reducing the scheme's effectiveness.

Several papers proposed different algorithms based on the principle of functioning above described in order to find the optimal point between selectiveness and detection capabilities. Thus, some authors combine the HD with other passive features to avoid false positive islanding diagnosis. In (JANG; KIM, 2004), (LAAKSONEN, 2013), (WANG, 2020), by the other side, is proposed a HD adaptation that combine the monitoring of the PCC voltage harmonic with the unbalance of voltage. The results reached correct islanding detection to balance and unbalance load conditions. Beyond that, it presented good results in terms of distinguishing islanding contingencies from other events. In (MLAKIĆ; BAGHAEE; NIKOLOVSKI, 2018) is proposed a approach that conjugates the HD philosophy with the Gibbs Phenomenon. The tests conducted demonstrated that this approach effectively detects islanding in multi-DG systems, with a smaller NDZ compared to passive HD methods and lower harmonic content than active AIP strategies.

Other solutions diagnosis an islanding event based on the individual components either than the THDv. In (LISERRE et al., 2006) the energy density of the fithty harmonic order is estimated using a Kalman filter. In (COLOMBAGE et al., 2017) is proposed an AIP solution based on the PWM harmonic signature of the inverter. This strategy uses high harmonic component orders, so it demands AIP devices that work with high sampling frequency. The reference (REIGOSA et al., 2017) proposes a HD passive islanding detection method based on the even harmonic and, in (ABDELSALAM et al., 2020), the islanding detection is obtained by applying a Discrete Fourier Transform to extract the second harmonic order of voltage and current.

3.4.4 Rate of Change of Frequency (ROCOF)

The Rate of Change of Frequency (ROCOF) based AIP strategies detect the grid interruption based on the derivative of frequency. The mathematical expression of the ROCOF is illustrated by (3.10). The ROCOF rate depends on some physical characteristics of the DGS, such as: inertia, nominal frequency and rated power and power-consumption unbalance according to (3.11) (CHOWDHURY; CHOWDHURY; CROSSLEY, 2009). The technique can

be realized using various methods, such as a Cross-Zero Detector (CZD), Fast Fourier Transform (FFT) (TEN; CROSSLEY, 2008), Phase Locked Loop (PLL) (DE LA O SERNA, 2015), Interpolated Discrete Fourier Transform combined with a Kalman Filter (SINGH; PAL, 2019), or through Phasor-Measurement Units (PMU) (FRIGO et al., 2019).

$$ROCOF = \frac{1}{n}\sum_{k=1}^{n}\frac{df}{dt}(k) \tag{3.10}$$

$$\frac{df}{dt} = \frac{\Delta P}{2HG}f \tag{3.11}$$

A significant challenge in ROCOF-based AIP lies in identifying the optimal measurement window to calculate ROCOF and establishing an accurate threshold to reliably detect grid According to (CHOWDHURY; CHOWDHURY; CROSSLEY, 2009), the time interval should be between 0.3 and 0.7 seconds, with the detection must be confirmed at 0.3 Hz/s. Additionally, (WANG; XIONG; WANG, 2019) introduces a methodology for configuring ROCOF relays based on a field study of a biomass power plant. Another challenge is coordinating the ROCOF relay with other frequency protection devices. To address this, (VIEIRA et al., 2006) applied a graphical design method to ensure coordination between Over-Under Frequency (OUF) relays and ROCOF relays.

A significant drawback of ROCOF is its possibility of false islanding detection due to motor starting or capacitor bank switching. Several studies have attempted to mitigate this by combining ROCOF with other electrical quantity monitoring. For instance, (TEN; CROSSLEY, 2008) employed an undervoltage interlock to guarantee selectivity between grid interruptions and voltage dips. In (LIU; THOMAS, 2011), ROCOF is locked to the THDi levels. (JIA et al., 2014) combined ROCOF with grid impedance estimation, while (GREBLA; YELLAJOSULA; HOIDALEN, 2020) enhanced ROCOF using an adaptive Kalman filter, which reduces sensitivity to non-islanding faults.

Despite its challenges, ROCOF offers several advantages. One is its versatility, as it can be applied to PV systems (LIU et al., 2016), in Synchronous Generator based systems (JIA et al., 2014) or in different types of microgrids (ALTAF et al., 2021). Furthermore, many active AIP methods incorporate ROCOF relays to speed up islanding detection. Examples include (AKHLAGHI et al., 2017), who combined SMS and ROCOF; (KHODAPARASTAN et al., 2017), who presented a hybrid method using SFS and ROCOF; and (RAIPALA et al., 2017)

who used a ROCOF relay in an RPV-based AIP. . There is also an active ROCOF relay, proposed in (GUPTA; BHATIA; JAIN, 2017).

ROCOF does not have an analitycal methodology for its NDZ. However, various studies have tried to define the ROCOF NDZ through simulation or real-time evaluation. For example, (ARGUENCE et al., 2017) carried out a computational analysis to chart the NDZ across various RLC loads, quality factors, and inertia constants of PV systems, demonstrating that the NDZ is influenced by load quality factors as well as the active and reactive power flow between the grid and the PCC. In another study, (ISA; MOHAMAD; YASIN, 2015) demonstrated that combining ROCOF with ROCOV relays results in a smaller NDZ than using OUF and OUV relays. Lastly, (ALAM; BEGUM; MUTTAQI, 2019) conducted a comprehensive computational study to determine the maximum boundary of the ROCOF NDZ.

3.4.5 Rate of Change of Voltage (ROCOV)

This method determines the Rate of Change of Voltage (ROCOV) since a grid interruption can cause a transient deviation in the PCC voltage (CHANG, 2011). Mathematically, the general implementation of the algorithm is expressed by (3.12):

$$ROCOV = \frac{\Delta(V_n - V_{n-1})}{\Delta t} \tag{3.12}$$

ROCOV can be used for islanding detection as well as for diagnosing other electrical contingencies. ROCOV can be applied to perform fault detection for High Voltage Direct Current (HVDC) systems (SNEATH; RAJAPAKSE, 2016), (PÉREZ MOLINA et al., 2020) or in DC microgrids (MAKKIEH et al., 2019). Additionally, this method can detect the loss of the main grid in AC microgrids, as reported by (BAKHSHI-JAFARABADI et al., 2021). ROCOV can also complement other AIP strategies. For example, (SEYEDI et al., 2021) proposed a hybrid approach that combines ROCOV and Rate of Change of Active Power (ROCOAP) to detect islanding in a multi-DG environment.

Furthermore, (DAWOUD et al., 2021a) concluded that ROCOV relays offer greater selectiveness and reliability compared to conventional current and voltage protection devices. (DAWOUD et al., 2021b) also proposed a coordination scheme for microgrids based on ROCOV measurements.

3.4.6 Rate of Change of Phase Angle Difference (ROCPAD)

The ROCPAD method, introduced by (SAMUI; SAMANTARAY, 2011), involves continuously monitoring the Rate of Change of the Phase Angle Difference (ROCPAD) between the inverter's output current and voltage, measuring the behavior of this difference over time. The mathematical representation is given by (3.13). In (ABYAZ et al., 2019) is proposed a passive AIP with ROCOF, ROCOV and ROCPAD monitoring to reduce NDZ.

$$ROCPAD = \frac{\Delta(\theta_{inv})}{\Delta t} \tag{3.13}$$

3.4.7 Other Rate of Change based methods

As mentioned earlier, islanding can cause sudden transient deviations in various electrical parameters, with frequency and voltage being the most commonly affected. The literature also discusses other derivative-based relays, such as the Rate of Change of Power (ROCOP)) (REDFERN; BARRETT; USTA, 1995), Rate of Change of Reactive Power (ROCORP) (ALAM; MUTTAQI; BOUZERDOUM, 2012), Rate of Change of Frequency over Power (ROCOFoP) (PAI; HUANG, 2001), and Rate of Change of Voltage over Power (ROCOVOP) (MAHAT; CHEN; BAK-JENSEN, 2009). Finally, (REDDY; REDDY, 2017) proposes a method that combines ROCOP e ROCOQ.

3.5 Local Active Methods

As previously mentioned, passive AIP operation can present large NDZ. To address the limitations caused by the NDZ in passive AIP methods, active anti-islanding solutions were developed. These active methods introduce perturbations into the inverter's operation to shift one PCC variable outside the operational threshold. Despite the power quality degradation associated with active solutions, they are widely adopted due to their superior performance when compared with passive solutions (DE MANGO et al., 2007b).

Active AIP methods can generally be categorized into three main groups: the first group introduces perturbations to the inverter's reactive power; the second group focuses on perturbing the active power; and the third group relies on harmonic injection techniques.

3.5.1 Active Frequency Drift (AFD) based methods

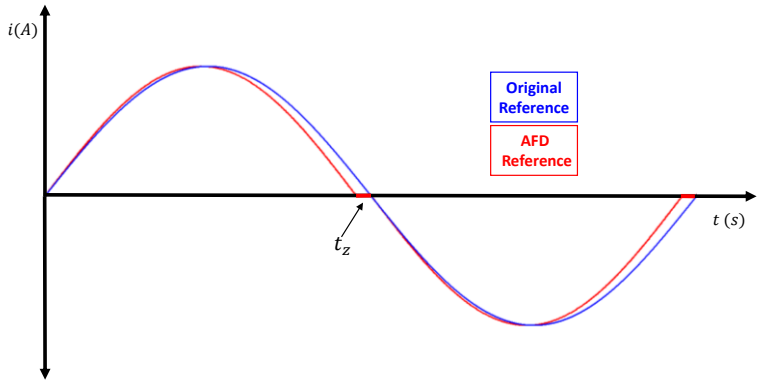
The Classic AFD, introduced by (ROHATGI, 1999), works by inserting a dead time at the end of each half-cycle, as illustrated in Figure 3.4. The philosophy of operation involves creating a zero-conduction period at the conclusion of each half-cycle, generating a phase shift between the PCC voltage and the inverter current output while maintaining the zero-crossing synchronization.The Classic AFD presents only one parameter, the chopping factor (c_f), defined according to (3.14) (RESENDE et al., 2019b).

$$c_f = \frac{2t_z}{T} \tag{3.14}$$

Mathematically, the wave exposed in Figure 3.4, is given by (3.15).

$$i_{afd}(t) = \begin{cases} Isin\left(2\pi\left(\frac{f}{1-c_f}\right)t\right), & 0 < \omega t \leq \pi - t_z \\ 0, & \pi - t_z < \omega t \leq \pi \\ Isin\left(2\pi\left(\frac{f}{1-c_f}\right)t\right), & \pi < \omega t \leq 2\pi - t_z \\ 0, & 2\pi - t_z < \omega t \leq 2\pi \end{cases} \tag{3.15}$$

Figure 3.4 – AFD distorted reference current.



Source: (RESENDE et al., 2019b).

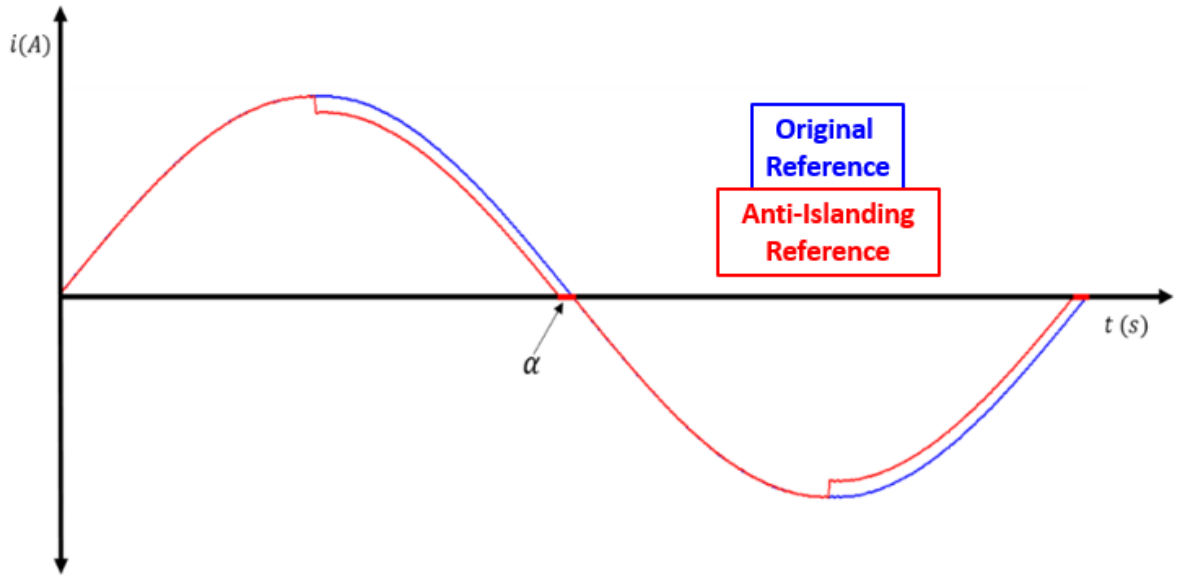
The primary advantage of the AFD solution is its simplicity of implementation. However, it is important to note several significant drawbacks: inefficiency in islanding detection for multi-DG systems, high levels of THDi, and pronounced NDZ challenges (RESENDE et al., 2019a). Additionally, the AFD has a fixed parameterization, which introduces operational issues related to frequency drift caused by the load. For example, when the coefficient c_f is positive, the AFD tends to shift the frequency above the nominal grid frequency. Conversely, with more inductive loads, the frequency tends to drift below 60 Hz. In such cases, the

frequency shift imposed by the AIP can be offset by the load-induced drift, potentially leading to a failure in detecting grid disconnection.

3.5.2 Improve Active Frequency Drift (IAFD)

To address the THDi issue of the Classic AFD, (YAFAOUI; WU; KOURO, 2010) proposed a modified version of the algorithm. In this improved approach, instead of introducing a dead time (t_z), a step change in the current magnitude is applied during the odd quarter-cycles of the current, as shown in Figure 3.5.

Figure 3.5 – IAFD distorted reference current.



Source: (RESENDE et al., 2019b).

Equation (3.16) represents the IAFD current waveform.

$$i_{iafd}(t) = \begin{cases} Isen(2\pi ft), & 0 < \omega t \leq \frac{\pi}{2} \\ Isen(2\pi ft) - KI, & \frac{\pi}{2} < \omega t \leq \pi - \arcsin(K) \\ 0, & \pi - \arcsin(K) < \omega t \leq \pi \\ Isen(2\pi ft), & \pi < \omega t \leq \frac{3\pi}{2} \\ Isen(2\pi ft) + KI, & \frac{3\pi}{2} < \omega t \leq 2\pi - \arcsin(K) \\ 0, & 2\pi - \arcsin(K) < \omega t \leq 2\pi \end{cases} \quad (3.16)$$

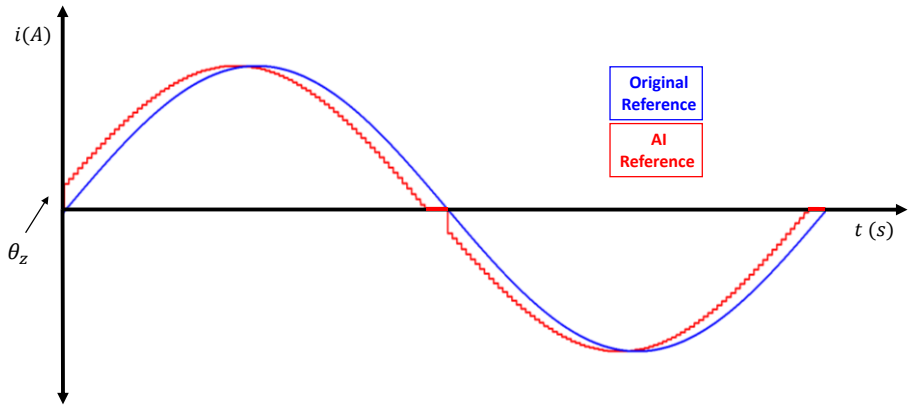
As one can see, the parameter K impacts on the level of intrusion of the IAFD algorithm. Additionally, the K gain affects the determination of the NDZ once it determines the phase difference between current and voltage, as described by equation (3.17).

$$\tan(\phi_{inv}) = \frac{2K}{\pi - 2K} \tag{3.17}$$

3.5.3 Active Frequency Drift by (CHEN et al., 2013).

In (CHEN; WANG; JIANG, 2013) is proposed an alternative version of the AFD algorithm. This strategy inserts the concept of active phase jump at the beginning of each half-cycle of current, as shown in Figure 3.6. Mathematically, the waveform depicted in Figure 3.5 can be expressed by equation (3.18).

Figure 3.6 – AFD by (CHEN; WANG; JIANG, 2013) distorted reference current.



Source: (RESENDE et al., 2019b).

$$i_{afd}(t) = \begin{cases} I_{pic} * sin(2\pi ft + \theta_z); \ 0 < \omega t \leq \pi - \theta_z \\ 0; \ \ \pi - \theta_z < \omega t \leq \pi \\ I_{pic} * sin(2\pi ft - \theta_z); \ \pi < \omega t \leq 2\pi - \theta_z \\ 0; \ 2\pi - \theta_z < \omega t \leq 2\pi \end{cases} \tag{3.18}$$

The phase difference between PCC voltage and inverter output current is given by (3.19).

$$\text{tg}(\phi_{\text{inv}}) = \frac{\pi - \theta_z}{1 + (\pi - \theta_z)\cot(\theta_z)} \tag{3.19}$$

3.5.4 Active Frequency Drift with Pulsating Chopping Factor (AFDPCF).

As previously discussed (see subsection 3.5.1), the Classic AFD cannot track the frequency drifting behavior caused by local loads once it presents fixed parametrization. To

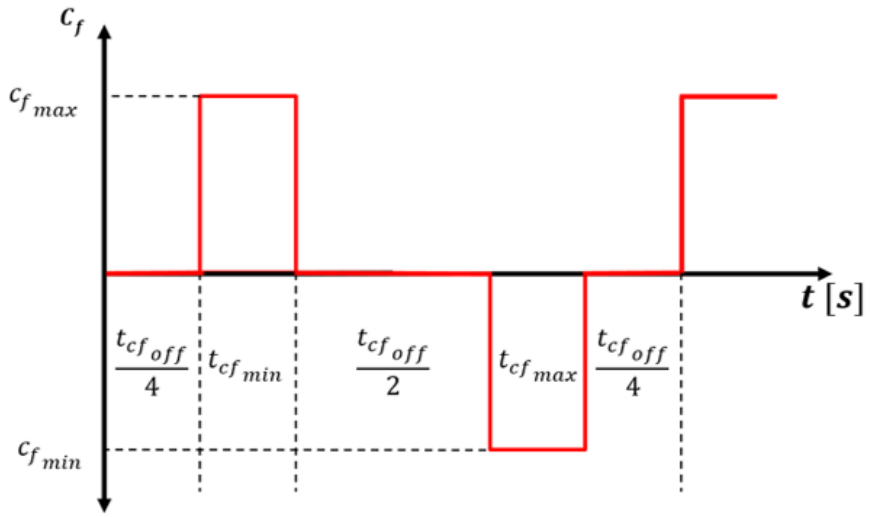
address this, (JUNG et al., 2005) introduced the AFDPCF, which replaces the fixed c_f value with a pulsating signal with positive, zero, and negative values, as defined by equation (3.20). Figure 3.7, in turn, illustrates the pulsating behavior of c_f over time

$$c_f = \begin{cases} c_{f\,max}; & if\ T_{cmax\ on} \\ c_{f\,min}; & if\ T_{cmin\ on} \\ 0; & if\ T_{coff\ on} \end{cases} \tag{3.20}$$

The most important advantage comes from the reduction of harmonic distortion of current due to the moments $c_f = 0$. Additionally, the alternation between positive and negative c_f values enables the algorithm to detect islanding regardless of the frequency deviation direction caused by local loads.

The AFDPCF algorithm effectively eliminates the NDZ for a range of Q_f values, as illustrated in Figure 3.7. Specifically, a $c_{f_{max}}$ of 0.2 eliminates the NDZ for $0 \leq Q_f \leq 1.61$, while a $c_{f_{max}}$ of 0.4 extends this range to $0 \leq Q_f \leq 3.2$. In (RESENDE et al., 2022), a design methodology was proposed for implementing the AFDPCF, which calculates the $c_{f_{max}}$ and $c_{f_{min}}$ values needed to eliminate a specified range of quality factor values. This methodology is represented by equation (3.21).

Figure 3.7 – c_f behavior after the AFDPCF implementation.

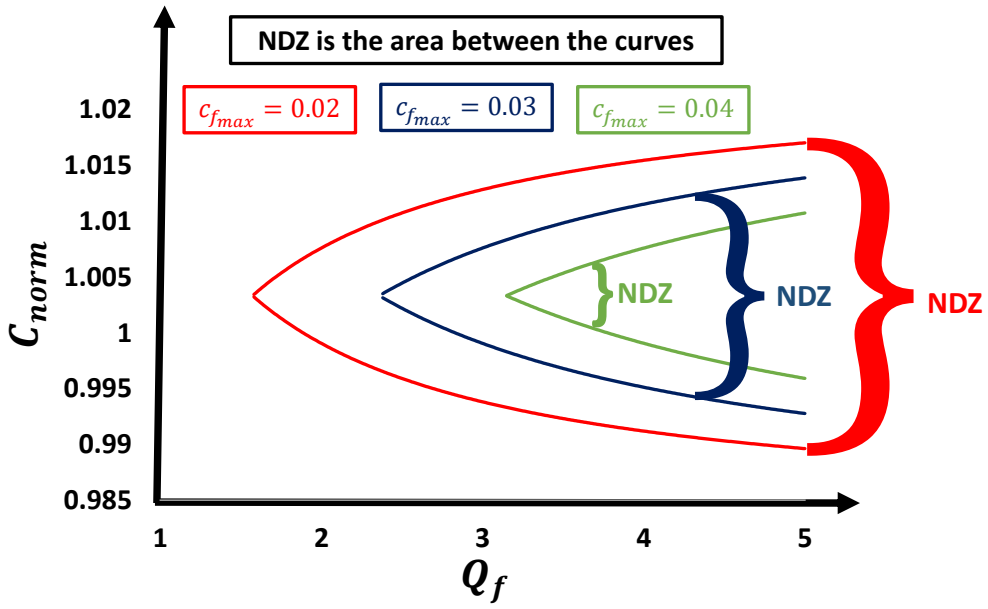


Source: (RESENDE et al., 2019a).

$$c_f = \begin{cases} c_{f\,max} = \dfrac{2.4Q_f}{f_0\pi} \\ c_{f\,min} = -c_{f_{max}} \end{cases} \tag{3.21}$$

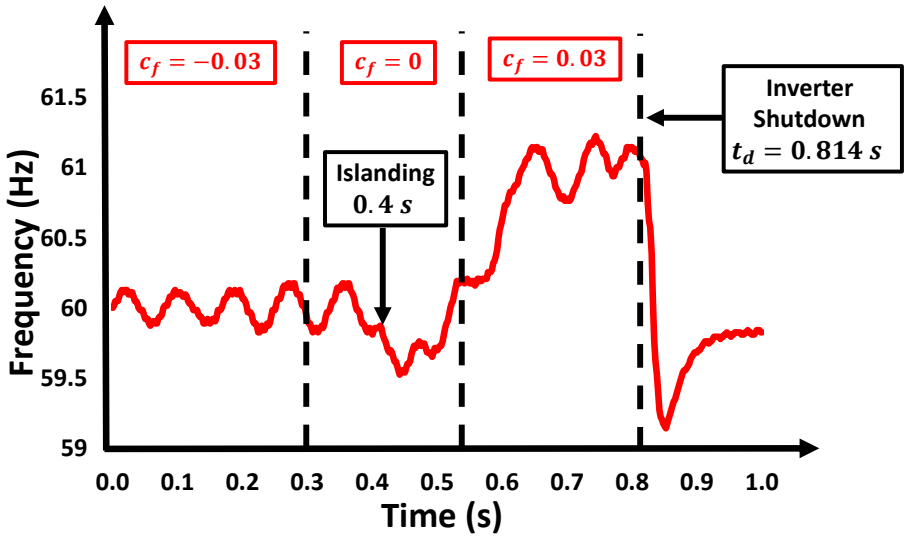
On the other hand, the primary disadvantage of the algorithm is its relatively long detection time. As highlighted in (RESENDE et al., 2022), there is no synchronization between the change in c_f value and the moment of grid disconnection. In this case, if islanding occurs when $c_f = 0$, the method can only initiate the frequency drift once c_f changes, as shown in Figure 3.9.

Figure 3.8 – AFDPCF NDZ for different values of c_{fmax}.



Source: (RESENDE et al., 2022).

Figure 3.9 – AFDPCF frequency result after an islanding occurrence.



Source: (RESENDE et al., 2022).

3.5.5 Sandia Frequency Shift (SFS)

The SFS algorithm was proposed by (ROHATGI, 1999) and positively feedbacks the frequency in the algorithm parametrization (3.22).

$$c_f = c_{f_0} + K(f_{pll} - f_n) \tag{3.22}$$

The phase difference between inverter current and PCC voltage after SFS implementation is shown in equation (3.23).

$$\theta_{inv} = \frac{\pi(c_{f_0} + K(f_{pll} - f_n))}{2} \tag{3.23}$$

The primary benefits of the SFS method include the reduction of THDi rates and the detection time (RESENDE et al., 2019a). During grid tie operation, the PLL measures a frequency nearly identical to the nominal grid frequency. Consequently, the frequency error is minimal, resulting in a low c_f value and a correspondingly low THDi rate in the inverter output current. However, if a grid interruption occurs, the frequency deviates from the nominal value, increasing c_f. This frequency deviation further amplifies cf, creating a feedback loop that shortens the detection time.

As observed, the SFS algorithm is controlled by the c_{f_0} and the accelerating gain K. While the c_{f_0} affects the THDi rate, the gain K determines the NDZ size (RESENDE et al., 2021). In (ZEINELDIN; KENNEDY, 2009a), is proposed a design methodology for choosing the value of K in order to eliminates the NDZ for a given interval of Q_f. The methodology is described by:

$$K > \frac{4Q_f}{\pi f_0} \tag{3.24}$$

The NDZ of the SFS can be affected by the number of inverters connected to the electrical island and the algorithm can present loss of effectiveness in this context. To address this, (VAHEDI; KARRARI; GHAREHPETIAN, 2016) introduced an alternative parameterization methodology to improve performance of the SFS for multi-inverter based DGS and microgrids. This methodology still needs real-time evaluation.

Paper (WANG; FREITAS; XU, 2011) examined the influence of the c_{f_0} and K on the NDZ mapping and size. It was discovered that K impacts the value of Q_f that do not present

NDZ, thus the increasing of K reduces the NDZ size. On the other hand, c_{f_0} determines the value of the C_{norm} at the initial point of the NDZ. On this basis, the growing of c_{f_0} implies on the increasing of the C_{norm}.

Nevertheless, (WANG; FREITAS, 2008), found that the accelerating gain K can lead inverter operation to instability, especially in weak grids or for large size DGS. In this scenario, (AL HOSANI; QU; ZEINELDIN, 2015) introduced novel approach based on the concept of the pulsating initial chopping factor, similar to the AFDPCF algorithm. The fixed value of c_{f_0} is replaced by a pulsating signal that alternates its value according to (3.25)

$$\boldsymbol{c_f} = \begin{cases} \boldsymbol{c_{f_0} = 0.05; K = 0.03\,, if\ T_1} \\ \boldsymbol{c_{f_0} = 0\,; K = 0.03\,, if\ T_2} \end{cases} \tag{3.25}$$

Another approach to parameterization involves the use of machine learning and artificial intelligence techniques to optimize the selection of the algorithm parameters. In (VAHEDI; KARRARI, 2013), for instance, is employed an adaptive fuzzy logic algorithm to perform SFS parameterization by estimating local load parameters and determining the minimum K value that eliminates the NDZ for the estimated conditions. Meanwhile, In (HATATA; ABD-RABOH; SEDHOM, 2018) used an immune system-based machine learning algorithm for parameterization. Their experimental results demonstrated qualitatively superior THDi and detection time in differente resources based DGS.

3.5.6 Slip Mode Shift (SMS)

The Slip Mode Frequency Shift (SMS) method introduces a small perturbation to the phase estimated by the PLL using a positive frequency feedback, as shown in equation (3.26). In this case, the inverter output current is described by equation (3.27) (TEODORESCU; LISERRE; RODRÍGUEZ, 2011).

$$\theta_{SMS} = \theta_M \sin\left(\frac{\pi}{2}\frac{(f - f_i)}{f_i - f_m}\right) \tag{3.26}$$

$$I_{inv} = \sqrt{2} I_{peak} \sin(2\pi f + \theta_{SMS}) \tag{3.27}$$

The main benefits of this AIP scheme include its ability to track load-induced frequency deviations, ease of digital implementation, and the elimination of the NDZ for a given Q_f factor (AKHLAGHI; AKHLAGHI; GHADIMI, 2016). In (LOPES; SUN, 2006) is conducted a comparative study on the impact of multi-DG islanding on the NDZ in the SMS strategy, finding that the method may result in a larger NDZ when operating alongside an inverter using the SFS algorithm.

In (HUNG et al., 2003) is introduced the Automatic Phase Shift (APS) algorithm, which applies an initial fixed perturbation to the θ_{SMS}. In (MOHAMMADPOUR et al., 2016) it is proposed a modified APS with dynamic parameters that change their values according to the load impedance. In (BIFARETTI et al., 2015) is suggested combining SMS with the ROCOF algorithm to reach faster islanding detection. In (AKHLAGHI; GHADIMI; AKHLAGHI, 2014) is developed a hybrid AIP that integrates SMS with the Q-f droop curve.. In (BRITO et al., 2018) SMS is compared with the SFS algorithm and presented faster islanding detection.

3.5.7 Sandia Voltage Shift (SVS)

The Sandia Voltage Shift (SVS) introduces a disturbance in the inverter's current reference, causing a voltage drift at the PCC after a grid interruption (CEBOLLERO et al., 2022). Its key advantage is the ability to detect islanding even when the load demand matches the power supplied by the SGD. Additionally, since the voltage of the electrical islanding with a inverter operating as a current source is less influenced by the grid's reactive power flow, the method is less affected by reactive power.

However, the primary drawbacks of SVS include power quality degradation and potential impacts on inverter stability (ZHENG et al., 2020). In order to improve SVS performance, (VAZQUEZ; VAZQUEZ; FEMAT, 2020) proposed a Modified Sandia Voltage Shift (MSVS) which uses an exponential function for determining the positive feedback gain. This method work well in parallel with the SFS (SILVA, 2016). In (BRITO et al., 2018), SVS achieved accurate islanding detection with minimal power quality disturbance, although it required more time to shut down the inverter.

3.5.8 Reactive Power Variation (RPV)

In (ZEINELDIN et al., 2006), is proposed a new AIP method which introduces small perturbations in the inverter reactive power inverter reference. (LIN et al., 2013) uses machine learning techniques to accelerate grid interruption detection; (GUPTA; BHATIA; JAIN, 2015)

introduces a solution involving perturbation of the dq reference frame, which maintains selectivity and avoids inverter tripping during non-islanding situations, even for grid configurations with high impedance values.

In (CHEN; LI; CROSSLEY, 2019), a hybrid anti-islanding method is introduced, using four passive criteria—voltage variation, voltage unbalance, ROCOF, and frequency variation—to determine the correct moment to apply the RPV disturbance. In (WANG, 2020), a new hybrid algorithm is proposed, featuring two passive indicators—voltage unbalance and THDi—along with an active bilateral reactive disturbance. This method improves the proposal of (CHEN; LI; CROSSLEY, 2019), by offering accurate islanding detection with a lower computational burden, as it only requires two variable measurements. However, its suitability for multi-inverter systems remains undefined. Finally, in (NARAGHIPOIUR et al., 2021) is proposed a modified Q-f droop curve-based AIP is proposed. Experimental validation shows that it effectively eliminates the NDZ for a range of quality factor values, avoids false inverter tripping, and performs well in multi-DG islanding scenarios.

In (ZHANG et al., 2013), a bidirectional intermittent RPV-based anti-islanding algorithm is introduced, with parameterization linked to the load's frequency resonance. Both (ZHANG et al., 2013; ZHU et al., 2013) and (ZHU et al., 2013) strategies presented detection capabilities degradation for electrical islanding with more than one inverter. Additionally, these strategies are not suitable for non-unity power factor inverters. Thus, (CHEN; LI, 2016) introduces an innovative RPV-based AIP method that applies two sets of reactive power disturbances, guaranteeing correct islanding detection for inverter with unitary or non-unitary power factor.

3.5.9. Harmonic Injection

This AIP method that utilizes Harmonic Injection disturb the inverter's current reference by introducing a specific harmonic order and frequency. After a grid interruption, this causes an increase in the corresponding voltage harmonic order due to the interaction between the inverter current and the local load impedance. Known also as harmonic component injection, impedance at specific frequency, harmonic amplitude jump, or high-frequency signal injection (CEBOLLERO et al., 2022), this approach's key advantage is that it operates independently of any imbalance between generated and consumed power (TEODORESCU; LISERRE; RODRÍGUEZ, 2011). However, a major limitation is the difficulty in setting a security threshold for islanding detection. The method also faces potential NDZ for loads with strong

filtering capabilities and may experience nuisance trips due to background distortion, instrumentation noise, or other non-islanding events.

A common approach for this AIP method involves injecting a harmonic component into the PLL's current reference. In this regard, (CIOBOTARU; TEODORESCU; BLAABJERG, 2006) proposed a new PLL based on Second Order General Integrator (SOGI). Later, (CIOBOTARU; AGELIDIS; TEODORESCU, 2008) presented an AIP that introduces a harmonic signal, which can be approximated by a double-frequency oscillation. Experimental results showed this approach could successfully detect islanding even for an RLC parallel load with $Q_f < 5$. In (VELASCO et al., 2011), a similar AIP method was introduced, where the second harmonic disturbance was measured using the Goertzel Algorithm (GA), reducing computational load by minimizing the required number of math operations. The GA is also applied in (JIA et al., 2018) in a method that introduces a 9th harmonic component. Experimental results showed effective islanding detection, although the 2% amplitude threshold for the 9th harmonic makes this method more vulnerable to nuisance trips than those based on lower-order harmonics (VALSAMAS et al., 2018).

In (CAI et al., 2013), an AIP is proposed specifically for three-phase inverters, which introduces two non-characteristic current harmonics to measure grid impedance. This approach addresses the issue of nuisance trips caused by instrumentation noise by incorporating a digital processing algorithm. Additionally, it can detect islanding even under power imbalance conditions. In (TEDDE; SMEDLEY, 2014), the authors use subharmonic injection to prevent disturbance filtering by capacitive loads. The results show that the method can detect islanding within the range of $0.33 \leq Q_f \leq 1.8$ and for $C_{norm} = [0.95: 1.05]$ under various levels of inverter active power. In (DHAR; DASH, 2016), an AIP scheme is proposed that uses feedback from the rate of change of voltage harmonics to reduce detection time. It also employs a binary tree classification algorithm to avoid nuisance trips.

The paper (VOGLITSIS et al., 2019) provides an in-depth analysis of the challenges faced by harmonic injection-based methods in multi-DG systems, considering both the current DG configuration and its potential for expansion. It introduces the concept of the Upgrade Factor (UF), which determines the amount of additional DER penetration a DG system can handle without compromising its islanding detection capabilities. The paper also presents a technique utilizing an external integrator to maximize the UF, thereby improving the reliability of harmonic injection AIP solutions.

In this context, compatibility issues of harmonic injection schemes in multi-DG systems are explored in (LIU et al., 2019), (LIU et al., 2022). The first paper concludes that the compatibility of harmonic injection schemes in multi-DG environments depends on maintaining a phase difference of [-π/2; π/2] between disturbances generated by each inverter unit. Beyond that it proposes an AIP solution based on the insertion of harmonic orders of frequency with high frequency. In the second paper, in turn, this solution is adapted for DG systems with grid-connected transformers.

Another challenge with harmonic injection methods is processing a single harmonic order. Commonly, strategies such as the Goertzel algorithm, DFT, or machine learning techniques are employed, which require complex mathematical operations. To reduce computational demand, some researchers have suggested using cross-correlation-based approaches. In (YU; MATSUI; YU, 2011), for instance, an AIP method is presented that detects grid disconnections by evaluating the correlation factor between the current-magnitude disturbance and the inverter output voltage. Although this method performs well, it does not account for the influence of grid parameters and may be affected by flicker issues and interactions with DC voltage control. In (VOGLITSIS; PAPANIKOLAOU; KYRITSIS, 2019), another AIP is proposed that injects a second-order harmonic current component, utilizing natural grid characteristics and removing the need to monitor the injected current. This method also has a small NDZ and works effectively in Module Integrated Converters (MIC), including those with pseudo DC links.

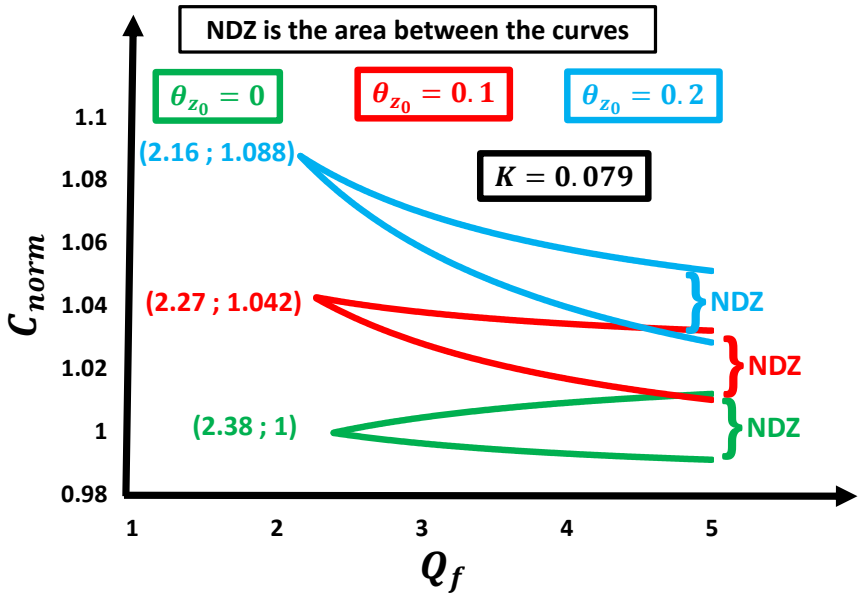
3.5.10. Active Phase Jump with Positive Feedback (APJPF)

In (RESENDE, 2020), a new anti-islanding solution called Active Phase Jump with Positive Feedback (APJPF) was proposed. This algorithm introduces frequency-positive feedback into the solution developed by (CHEN; WANG; JIANG, 2013), combining the advantages of both methods to reduce the NDZ and improve detection time. The value of $\boldsymbol{\theta_Z}$ is given by (3.28), in which the variable $\boldsymbol{f}$ represents the nominal grid frequency.

$$\theta_z = \theta_{z_0} + K(f_{pll} - f) \tag{3.28}$$

The algorithm performance depends on two parameters: $\boldsymbol{\theta_{z_0}}$ and $\boldsymbol{K}$. To better understand the parameterization of the APJPF algorithm, it's crucial to examine how each parameter affects NDZ mapping. Figure 3.10, therefore, illustrates the effect of $\boldsymbol{\theta_{z_0}}$ on NDZ.

Figure 3.10 – Influence of θ_{z_o} at the APJPF NDZ mapping.

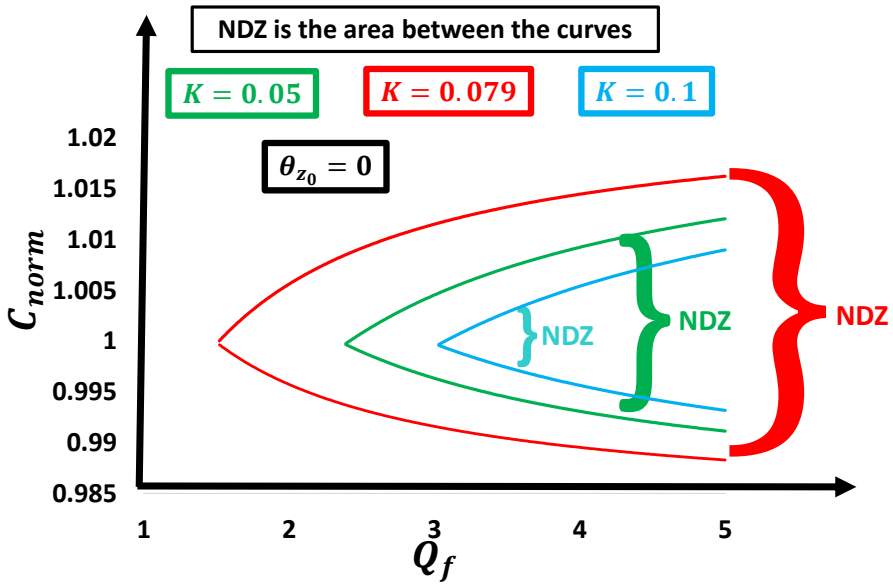


Source:(RESENDE et al., 2022).

As can be seen , for the same value of $\boldsymbol{K}$ and different values of $\boldsymbol{\theta_{z_o}}$ the value of $\boldsymbol{C_{norm}}$ is directly affected, so that the growing of the $\boldsymbol{\theta_{z_o}}$ also represents the growing of the value of $\boldsymbol{C_{norm}}$ at the initial point of the NDZ, which is a very positive fact. However, it is also possible to notice that the increasing of the $\boldsymbol{\theta_{z_o}}$ affects negatively the interval of quality factor for which the APJPF eradicates the NDZ, so that the increasing of $\boldsymbol{\theta_{z_o}}$ represents the decreasing of $\boldsymbol{Q_f}$ at the initial point of the NDZ, which is a very negative fact.

Once the influence of θ_{z_o} is well determined, it is important to understand the role of the gain K. Hence, the Figure 3.11 illustrates the APJPF NDZ for different values of K and a constant $\theta_{z_o} = 0$.

Figure 3.11 – Influence of K at the APJPF NDZ mapping.



Source: (RESENDE et al., 2022)

As can be seen , the growing of the K does not affect the value of C_{norm} at the initial point of the NDZ that, for all the conditions, was fixed in $C_{norm} = 1$. However, the value of Q_f was directly influenced by K hence the biggest is the chosen gain, the biggest is the value of the quality factor at the beginning of the NDZ and, consequently, the lower is the NDZ size.

The work (RESENDE et al., 2022) exposes that the θ_{z_o} has a bigger impact on the THDi than the accelerating gain. Based on that, it is proposed a design methodology for the APJPF that goals to achieve the biggest NDZ reduction with the lowest THDi demanded, expressed by (3.29). Instructions for the correct choosing of σ is given in (RESENDE et al., 2022).

$$\boldsymbol{\theta_z} = \begin{cases} \boldsymbol{\theta_{z_o} = 0} \\ \boldsymbol{K > \dfrac{Q_{f_{APJPF}} + 0.11702}{31.91489} + \sigma} \end{cases} \tag{3.29}$$

Where:

- $Q_{f_{APJPF}}$ – Quality factor of the NDZ initial point;
- σ – Correction factor;

3.5.11. Active Phase Jump with Positive Feedback and Intermittent Perturbation (APJPFIP) – Proposed Method

As it was demonstrated by the literature review, the AIP schemes based on the distortion of the inverter output current are able to perform the islanding detection accurately due to the modern improvements they have received over the past years.

In spite of the high THDi levels of the Classic AFD, (YAFAOUI; WU; KOURO, 2010) and (CHEN; WANG; JIANG, 2013) proved that with different current waveforms perturbation it is possible to reduce the harmonic content demanded by the AIP without losing efficiency. The insertion of a positive feedback in the design of an AIP is able of mitigating THDi and eliminating the NDZ for a given range of Q_f. Furthermore, positive feedback-based algorithms can follow the frequency drifting tendency imposed by the local loads. Based on that, (RESENDE, 2020) proposed a new anti-islanding solution called Active Phase Jump with Positive Feedback (APJPF). This algorithm inserts a frequency positive feedback on the solution proposed by (CHEN; WANG; JIANG, 2013), amalgamating the main advantages of the two methods. The APJPF experimental validation, in (RESENDE et al., 2022), achieved a better performance than other popular AIP strategies: AFD, AFD by (CHEN; WANG; JIANG, 2013), AFDPCF and SFS for different load conditions.

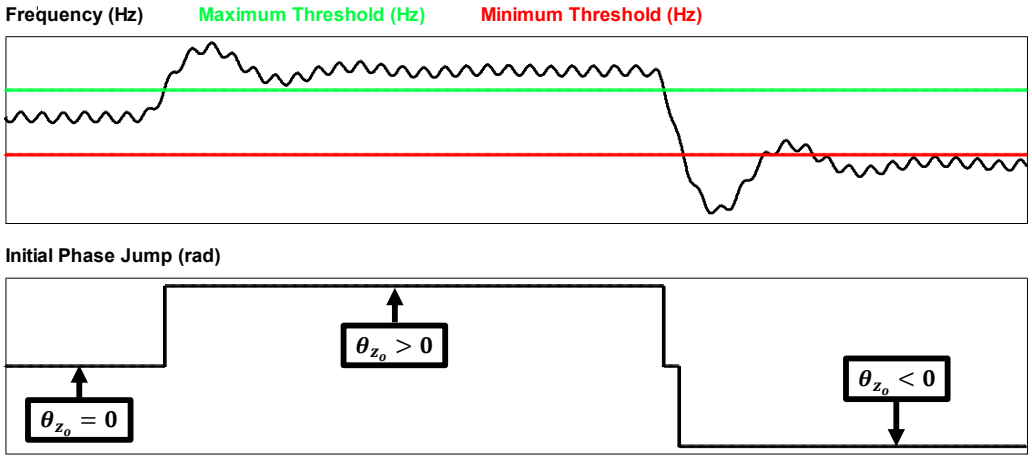
However, the main drawback of this kind of solution is the effect of the positive feedback gain on the inverter stability. If, by one hand, this variable is linked to the NDZ reduction, as proved by Figure 3.10, on the other hand, stability issues are the great barrier for the growing of the gain value. One way to address this is to use scheduled perturbation in one of the parameters of the AIP method. In this context, (AL HOSANI; QU; ZEINELDIN, 2015) proposed a modified version of the SFS algorithm with a schedule perturbation of the initial chopping factor, that alternates its value according to (3.25). The results, as aforementioned, showed a mitigation of the NDZ without the growing of the accelerating gain. Other schemes that successfully used schedule perturbation are the RPV based AIP proposed in (ZHU et al., 2013) and the AFDPFC. In the view of the foregoing, the main objective of this work is to present a new active anti-islanding protection that integrates the concepts of the frequency positive feedback and the scheduled perturbation.

As well as the project criterion proposed in (ZEINELDIN; KENNEDY, 2009b) for the SFS algorithm, the design methodology exposed in (3.28), for the APJPF, has two merits. The first one is the determination of the minimum value of K to eliminate NDZ and the second one

is to eliminate the θ_{z_o} parcel and, consequently, mitigate the THDi associated to the APJPF implementation. However, it is important to state that the fraction θ_{z_o} has the power to provoke a huge frequency drift, accelerating the islanding detection.

In this sense, the method proposed by this thesis goals to keep the value of $\theta_{z_o} = 0$ during the grid connected operation for mitigating THDi and step its value if the AIP suspects the grid has been interrupted to improve islanding detection. Thus, beyond determining a maximum and a minimum frequency threshold to perform the islanding detection, it will be also chosen a range of frequencies in which $\theta_{z_o} = 0$, such that, outside this interval, this parameter is staggered to either a positive or a negative value, according to the frequency drift tendency imposed by the local load. The Figure 3.12 presents the θ_{z_o} behavior for a positive and for a negative frequency step. As can be seen , after surpassing the maximum threshold the parameter becomes positive and, after reaching the minimum frequency threshold, negative.

Figure 3.12 – Behavior of $\boldsymbol{\theta_{z_o}}$ according to the measured of frequency.



Source: Author.

Mathematically, the value of the θ_{z_o} can be described by:

$$\boldsymbol{\theta_{z_o}} = \begin{cases} \boldsymbol{\theta_{z_o} > 0}; & \boldsymbol{f > f_{\theta max}} \\ \boldsymbol{\theta_{z_o} = 0}; & \boldsymbol{f_{\theta min} < f < f_{\theta max}} \\ \boldsymbol{\theta_{z_o} < 0}; & \boldsymbol{f < f_{\theta min}} \end{cases} \tag{3.30}$$

- $f_{\theta max}$ – The maximum frequency alarm threshold for the positive step of θ_{z_o};
- $f_{\theta min}$ – The minimum frequency alarm threshold for the negative step of θ_{z_o};

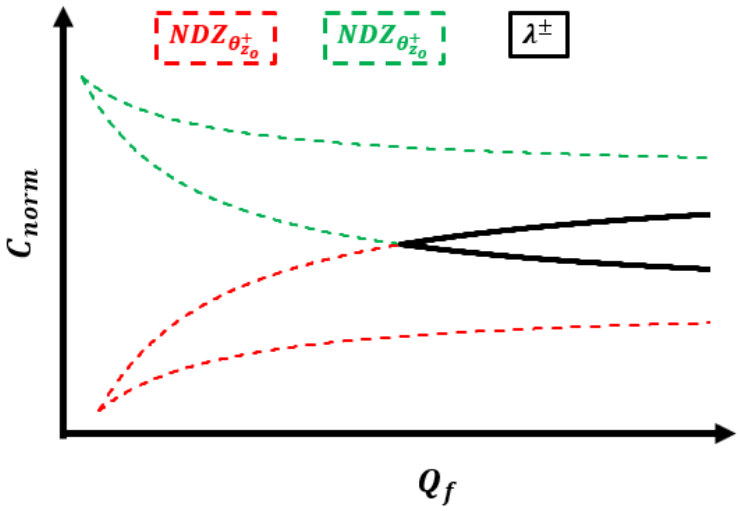
In order to understand the potentiality of the proposed scheme it is important to determine its NDZ. In this sense, it is necessary to state that, as the parcel θ_{z_o} alternates between a positive or a negative value after the frequency trespasses the thresholds $f_{\theta\,max}$ and $f_{\theta\,min}$, the APJPFIP NDZ contemplates the set ($\lambda^{\pm}$) that is the intersection between the APJPF NDZ for $\theta_{z_o} > 0$ and for $\theta_{z_o} < 0$, as described by 3.29. Figure 3.13, on its hand, shows the graphical representation of a generic $\lambda^{\pm}$ set.

$$\boldsymbol{\lambda^{\pm} = NDZ^{+} \cap NDZ^{-}} \tag{3.31}$$

Where:

- NDZ^{+} – The NDZ for $\theta_{z_o} > 0$;
- NDZ^{-} – The NDZ for $\theta_{z_o} < 0$;

Figure 3.13 – Graphical representation of the $\boldsymbol{\lambda^{\pm}}$ set.



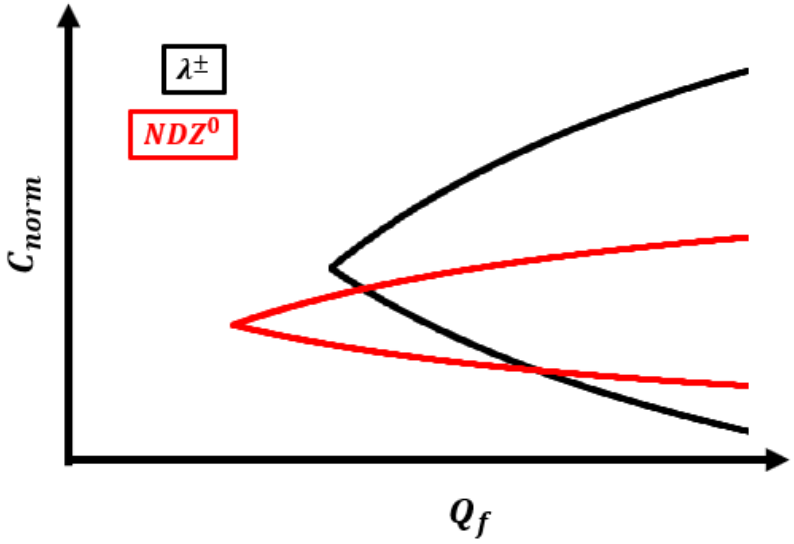
Source: Author.

It is easy to understand that the proposed method is unable to detect the islanding occurrence for all load conditions that belongs to the $\lambda^{\pm}$ set. However, as it was afore-mentioned, the main idea behind the proposed scheme is to keep $\theta_{z_o} = 0$ during the grid-connected operation and only step the initial phase jump through the trespassing of the frequency alarm thresholds. In this sense, one can see that the APJPFIP will also not be able to perform a positive islanding diagnosis if the local load is inside the NDZ of $\theta_{z_o} = 0$. Thus, the APJPFIP will be the union between the $\lambda^{\pm}$ set and the NDZ^{0}, that is the APJPF NDZ for $\theta_{z_o} =$

0 and related to the frequency alarm thresholds, as mathematically expressed by (3.32). In order to facilitate the comprehension, Figure 3.14 shows, separately, the graphical representation of the $\lambda^{\pm}$ and of NDZ^{0} and Figure 3.15 the graphical representation of the $NDZ_{APJPJIP}$, i. e., the union between the two afore-mentioned sets.

$$\boldsymbol{NDZ_{APJPJIP} = \lambda^{\pm} \cup NDZ^{0}} \tag{3.32}$$

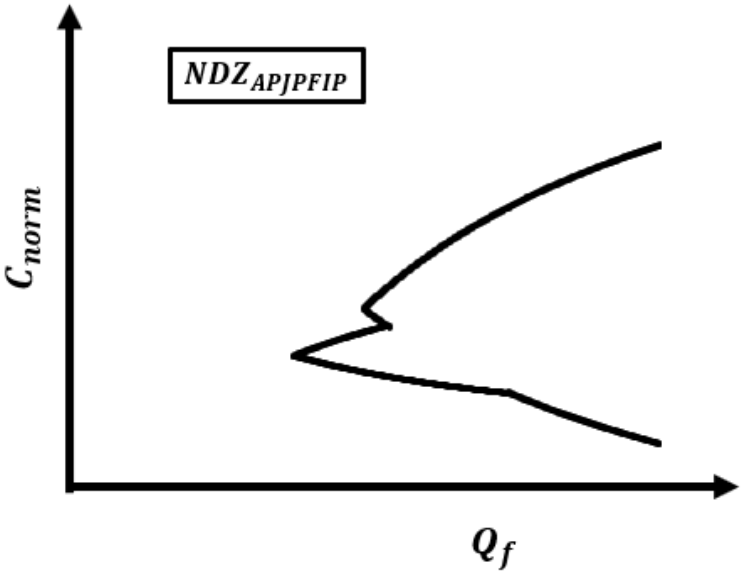
Figure 3.14 – Graphical representation of the $\lambda^{\pm}$ and NDZ^{0} sets, separately.



Source: Author.

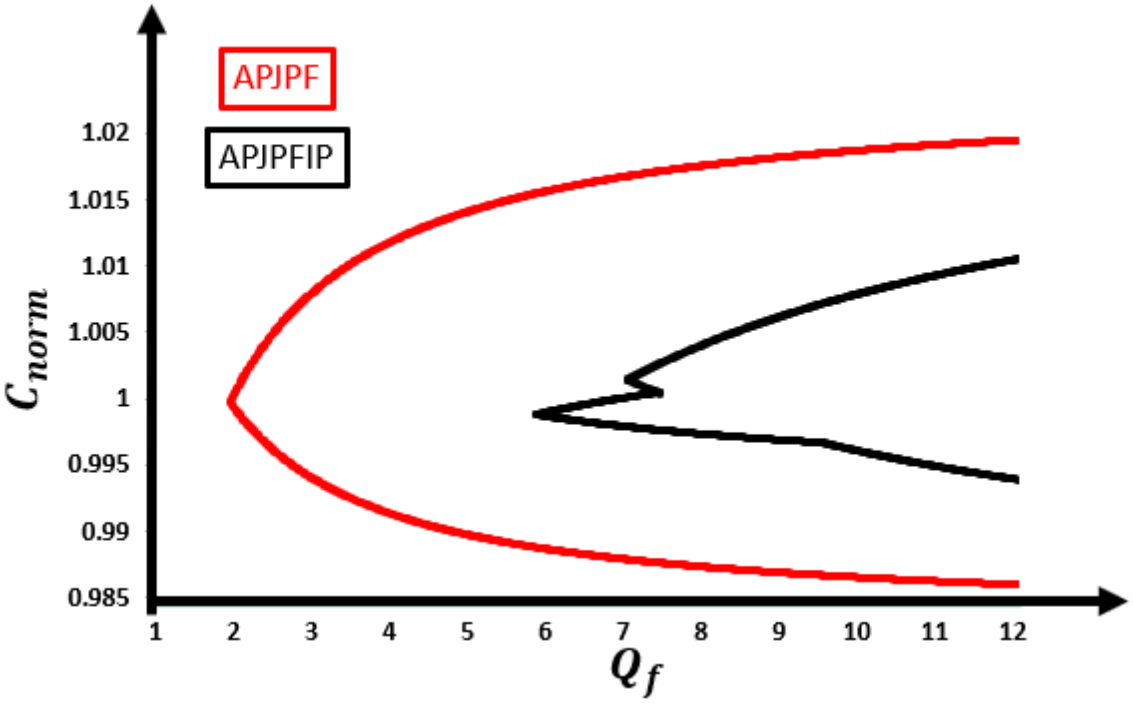
Finally, the Figure 3.16 presents the comparison between the NDZ of the APJPF and the APJPFIP for the same accelerating gain. For the APJPFIP, were chosen the following parameters: $f_{\theta\,max} = 60.2\,Hz$; $f_{\theta\,min} = 59.8\,Hz$; $\theta_{z_o}^{+} = 0.1$; $\theta_{z_o}^{-} = -0.1$; $K = 0.065$. For the APJPF, on its hand, were chosen: $= 0.065$; $\theta_{z_o} = 0$. As can be seen , the proposed strategy is capable of eliminating the NDZ for $0 \leq Q_f \leq 7.49$, while the APJPF, for the same value of K, abolishes the NDZ for $0 \leq Q_f \leq 2.12$.

Figure 3.15 – Graphical representation of $NDZ_{APJPFIP}$.



Source: Author.

Figure 3.16 – Graphical representation of $NDZ_{APJPFIP}$.

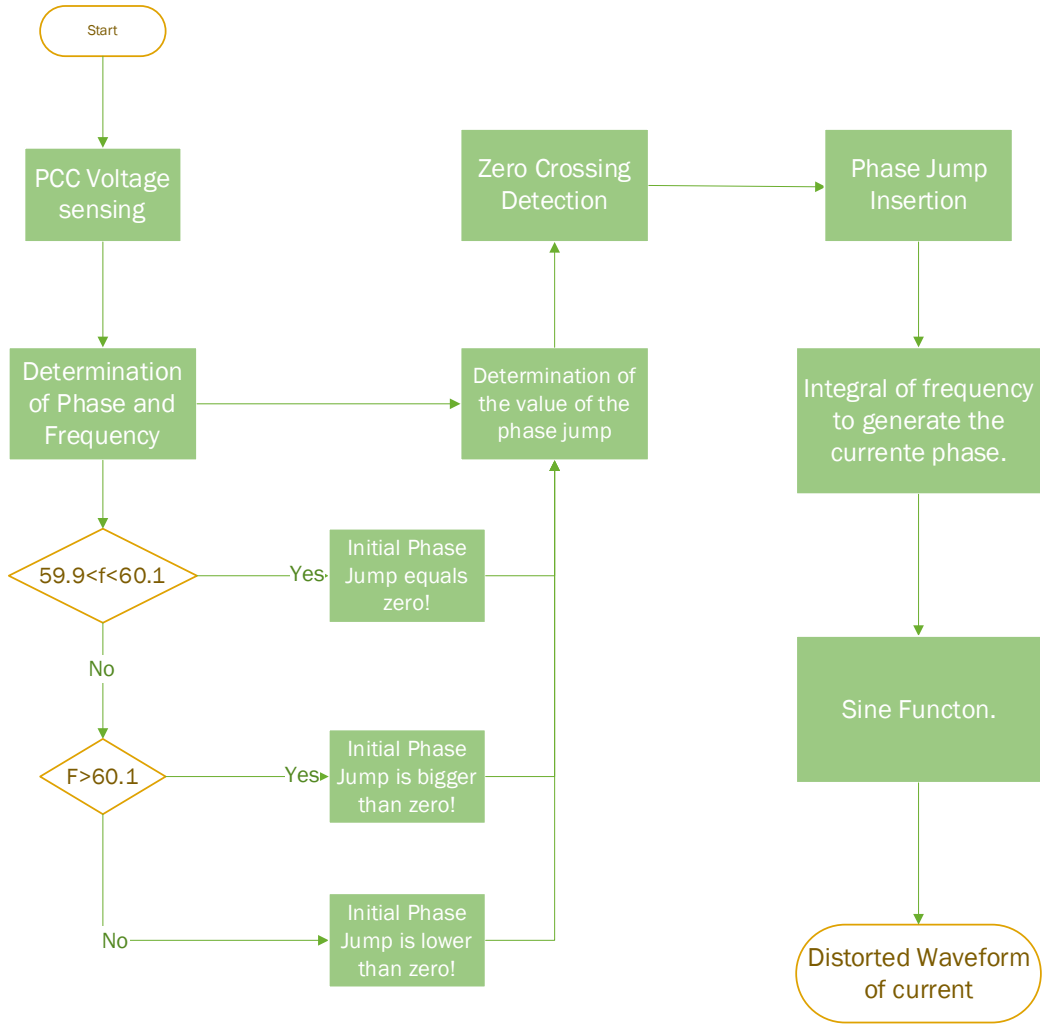


Source: Author.

Finally, Figure 3.17 presents the flowchart for the correct development of the proposed method, following the previously explained implementation methodology. The routine begins with sensing the PCC voltage, after which the sensed values are processed through a PLL that

extracts phase and frequency information. Next, the frequency is used to determine the value of θ_{z_0} according to equation 3.30. Subsequently, the frequency is fed back for determining the frequency error. The frequency error and phase are then input to the block "Determination of the Value of the Phase Jump," which calculates the disturbance value according to equation 3.28. After this, a Zero Crossing Detector signals the beginning of each half-cycle, and the perturbation is applied. Finally, an integrator determines the disturbed phase, and a sine function completes the process to obtain the distorted current waveform.

Figure 3.17 – Flowchart of the proposed method implementation.



Source: Author.

3.6 Final Considerations

The islanding phenomenon is defined by the electrical supply of local loads by a DGS even after grid interruption. The islanding may be caused by the intentional disconnection of

the grid to perform maintenance procedures, the non-intentional interruption of the grid in virtue of an external contingency, human mistake or sabotage and can lead to electrical accidents, equipment damage, degradation of power quality and/or out of phase reclosure. In virtue of its extremely negative potentiality, several Standards addresses the AIP as a mandatory feature for the connection of a DGS into the main utility grid. All Standard's recommendations requires an AIP to be tested under the most adverse load conditions.

In order to perform the grid interruption detection, different strategies have been proposed and it is possible to categorize them according to its location and to its philosophy of operation. According to the location, the AIP solutions can be divided in remote or local. While the remote techniques are based on the grid-side, the local solutions are, in general, embedded into the inverter microprocessor. In spite of its reliability, the remote methods are still expensive, demanding dedicated communication links and, therefore, are not recommended for small or medium DGS. The local solutions, on the other hand, are low-cost strategies. Their complexity of implementation has been reduced over the past years in virtue of the developments of the digital control technologies and, therefore, are in the state-of-the-art of islanding detection.

The local passive methods do not insert any disturbance on the electrical parameters. Otherwise, they determine the islanding occurrence by monitoring electrical variables at the PCC. The analyzed passive strategies were: OUF/OUV, phase jump detection, harmonic detection, ROCOF, ROCOV and ROCPAD. The active solutions, in turn, insert small disturbances on the inverter parameters to drift the operational point to out of the allowed values of operation. This chapter covered the main theory of operation of the following strategies: AFD, IAFD, AFD by (CHEN; WANG; JIANG, 2013), SFS, SVS, SMS, harmonic insertion, APJPF. Additionally, it was also exposed the philosophy of operation of a new active anti-islanding technique called APJPFIP.

The proposed scheme is based on the APJPF and that combines the concepts of the frequency positive feedback and the intermittent perturbation of the initial phase jump (θ_{z_o}). The main goal is to keep the value of $\theta_{z_o} = 0$ during the grid connected operation for mitigating THDi and step its value if the AIP suspects the grid was interrupted to improve islanding detection. Beyond that, it is expected that the scheme will be able to perform the islanding detection with a lower accelerating gain when compared to other positive frequency feedback-based islanding schemes.

Finally, the next chapter will cover the computational realization of the inverter and of the other anti-islanding strategies that will compose the comparative study. Beyond that, it will explain a new methodology of AIP test that will contemplate the most restrictive Standards recommendation. It will present results for two environments: a single inverter islanding and for a multi-DG system, under different values of quality factor and for different normalized capacitances.

CHAPTER IV

Computational Analysis Using Psim® Software

4.1 Introduction

This chapter aims to present the power and control structures utilized for validating the proposed AIP technique, along with a comparative study conducted in two scenarios. In the first scenario, the methods will be tested during an islanding event in a single-inverter DGS. The second scenario involves detecting islanding in a dual-inverter environment, designed to evaluate the capability of the APJPFIP to operate in parallel with other established AIP strategies. PSIM® software was used for these simulations. Additionally, the methodology for evaluating the methods and the results from the anti-islanding tests will be discussed. The comparison criteria for the results include total harmonic distortion of the current (THDi) and detection time.

4.2 Hardware and Control Setup

The power structure follows the setup recommended by the Standards and exposed in Figure 2.4. An LCL filter was used to mitigate harmonic distortion in the inverter's output current. The RLC load was designed in accordance with the recommendations of the standards (IEEE, 2000; IEEE, 2003). In this setup, the resistive parameter was calculated to match the inverter's rated active power, and the LC pair was tuned to resonate at the grid's nominal frequency, following equations (2.7), (2.8), and (2.9).

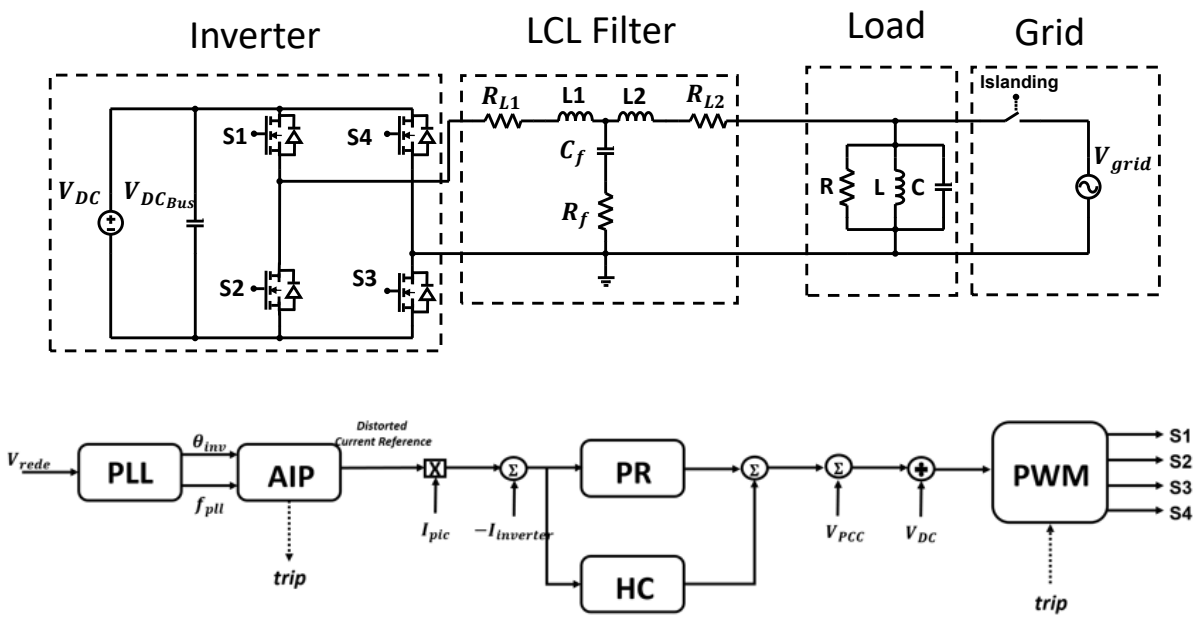
The peak of current is calculated. Subsequently, a SOGI-PLL was used to provide an in-phase sinusoidal current reference. This choice was based on the findings of (JUNIOR et al., 2019), which concluded that this synchronization technique can track phase and frequency deviations while providing accurate real-time frequency data with minimal oscillations.

The phase and frequency information is then fed into the AIP block, which generates the distorted reference required by each of the tested AIP schemes. It is worth noting that will be implemented six methods of islanding detection. In this sense, the output of this block will vary from each experiment. For the AFD, the output will be the waveform illustrated by Figure 3.4. For the AFD by (CHEN et al., 2013) the waveform illustrated by Figure 3.6. For AFDPCF the

output will be the waveform illustrated by Figure 3.4 but with c_f will present the same behavior demonstrated by Figure 3.7. For the SFS, it will be the waveform illustrated by Figure 3.4 with c_f varying according the positive feedback expressed by equation 3.22. For the APJPF it will be the waveform illustrated by Figure 3.6 but the phase jump will vary according the positive feedback expressed by equation 3.28. Finally, for the proposed method (APJPFIP) the output will result from the computational routine expressed by the flowchart of Figure 3.17.

The AIP block's output is multiplied by the current peak to generate the distorted current reference. The current control loop receives the error between the sensed value and the reference. The mitigation of the current error is done by a proportional resonante control equipped with harmonic compensators for the third, fifth, and seventh orders. Feedforward control utilizes the PCC voltage to enhance disturbance rejection, while feedback from the DC bus voltage ensures compensation for the inverter's static gain.

Figure 4.1 – Inverter power and control structure.



Source: Adapted from (RESENDE, 2020)

The chosen modulation method was a conventional unipolar sinusoidal PWM at 10 kHz, with DC bus voltage feedback to adjust the inverter's static gain. This unipolar PWM generates the semiconductor switching pulses. Additionally, an internal "Islanding" signal remains high during grid connection and switches to low to simulate islanding conditions, while the "Trip" signal changes from high to low upon islanding detection, disabling the PWM and shutting

down the inverter. Both power and control structures are shown in Figure 4.1.Finally, Table 4.1 presents the parameters of the inverter, the local load and for the utility grid.

Table 4.1 – Parameters of the grid, inverter and local load during the AIP tests.

Grid	
Rated Voltage	127 Vrms
Nominal Frequency	60 Hz
Inverter	
Output Voltage	127 V
Output Current	7.89 A
Rated Power	1000 W
First Filter Inductor	1.5 mH
First Inductor Resistance	0.05 Ω
Second Filter Inductor	10.5 mH
Second Inductor Resistance	0.05 Ω
Damping Resistor	2 Ω
Filter Capacitor	30 µF
Switching Frequency	10 kHz
Load	
Type	Parallel RLC
Total Resistance	16.129 Ω
Total Inductance	42.48 mH
Total Capacitance	164.5 µF
Resonance Frequency	60.05 Hz

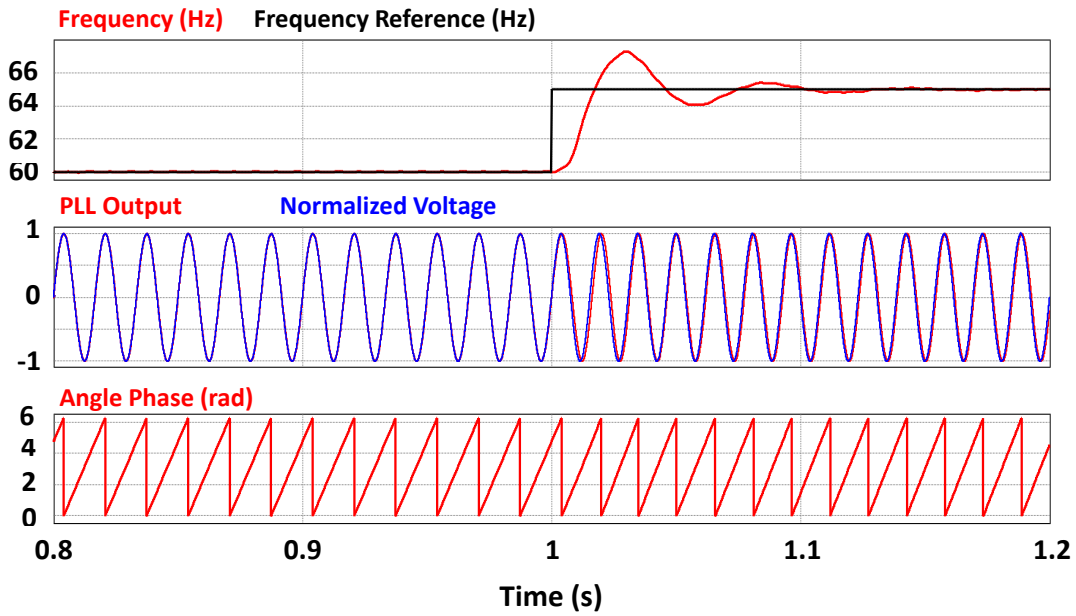
Source: Author.

4.3 SOGI Phase Locked Loop (SOGI - PLL)

Active AIP depends on phase and frequency data from the PLL, making PLL design crucial. Effective PLL features include tracking amplitude, phase, and frequency changes and providing stable frequency data with minimal oscillation. A study by Souza et al. (2019) found that the SOGI-PLL meets these needs. To correct phase error, either a PI controller or a low-pass filter can be used; a low-pass filter, selected here, minimizes frequency ripple and improves AIP performance, especially for methods sensitive to frequency errors, like SFS, APJPF, and APJPFIP. The filter's cutoff frequency was set to 1.2 Hz.

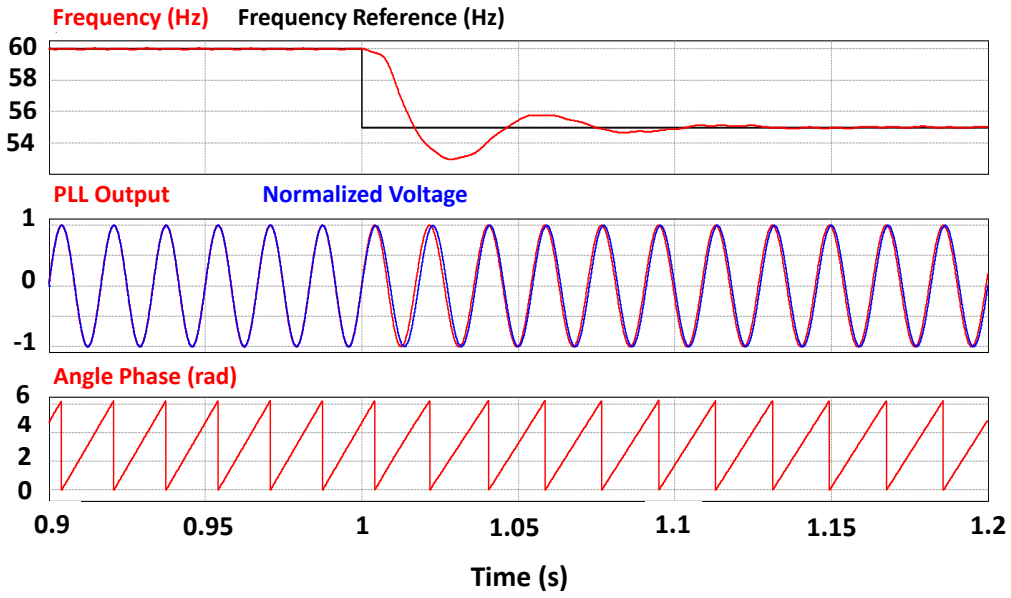
Figure 4.2 shows the frequency, synchronization, and phase results for a +5 Hz frequency step, while Figure 4.3 presents the same results for a -5 Hz variation. As can be seen, even under instantaneous variations of ±5 Hz, the designed SOGI-PLL can accurately calculate the frequency value. During grid following mode it was verified a ripple of 0.1 Hz. Additionally, the settling time is 0.1 seconds.

Figure 4.2 – Response of the PLL after a +5 Hz frequency variation.



Source: Author.

Figure 4.3 – Response of the PLL after a -5 Hz frequency degree.



Source: Author.

4.4 Passive Method Design

Active AIP operates by introducing small disturbances to an inverter parameter, pushing its operational point outside the limits specified by Standards. However, the actual inverter shutdown relies on a passive method, which must work in tandem with the active approach.

In this case, the chosen passive AIP method is OUF. This approach uses frequency data from the PLL, and when an irregularity is detected, a counter initiates. Once the counter starts, the inverter remains operational until the counter reaches a value of 1, at which point the control system triggers a shutdown signal. The counter calculation is described in equation (4.1). Adding a counter before the shutdown signal provides selective protection by ensuring that temporary frequency variations are not mistaken for an islanding event. The counter limit is set at 0.7, the strictest detection time referenced in the regulatory guidelines discussed. The T_s portion is equal to the sampling time and guarantees that the detection time is always less than or equal to that stipulated by the Standards. Finally, the $k_{ai} * |\varepsilon_{freq}|$ has the function of linking the detection time to the frequency deviation imposed by the active method. The k_{ai} parameter was experimentally calculated to avoid inverter shutdown in transient frequency variations.

$$t_n = t_{n-1} + T_s + k_{ai} * |\varepsilon_{freq}| \tag{4.1}$$

Where:

- t – counted time;
- T_s – Sample Time;
- k_{ai} – counter gain;
- ε_{freq} – frequency error;

4.5 Methodology

As previously mentioned, this work aims to compare the proposed anti-islanding technique with other well-known methods found in the literature: AFD, AFD by (CHEN et al., 2013), SFS, AFDPCF, and APJPF. The implemented methods performance will be compare according NDZ, THDi, and detection time.The NDZ of each method will be mapped in the $Q_f \; x \; C_{norm}$ plane for a range of quality factors varying from 0 to 10. Subsequently, the THDi results achieved by each method when operating at full load in grid-connected operation will be presented.

To determine the detection time, the analyzed methods will first be tested under an islanding contingency using a single inverter-based DGS. In this scenario, each strategy will be tested for three different values of the quality factor and eleven different values of normalized capacitance, totaling 33 tests. The chosen values of the quality factor are shown in Table 4.2, which also contains the justification for each one. For each value of Q_f, the normalized

capacitance will vary from 0.95 to 1.05 in increments of 0.01, according to the recommendations of IEEE 2003 and IEC 2014.

Table 4.2– Adopted quality factor

Quality Factor	Justification
1	According to the recommendations of IEEE 2003 and IEC 2014
2.5	According to the recommendations of IEEE 2000
5	In order to analyze each methods behavior in a rare and extremely adverse condition;

Source: Author.

Finally, Table 4.3 exposes the chosen parameters for each method.

Table 4.3– Analyzed AIP strategies and the chosen parameters.

AIP method	Parameter
AFD	$c_f = 0.032$
AFD by (CHEN et al., 2013)	$\theta_z = 0.1$
AFDPCF	$c_f = 0.045$
	$c_f = -0.045$
	$t_{max} = 0.3\ s$
	$t_{min} = 0{,}3\ s$
	$t_{off} = 0.4\ s$
	$c_f = 0.025$
SFS	$c_{f_o} = 0$
	$k = 0.904$
APJPF	$\theta_{z_o} = 0$
	$K = 0.14$
APJPFIP	$f_{\theta max} = 60.1$ Hz
	$f_{\theta min} = 59.85$ Hz
	$\theta_z^+ = 0.1$
	$\theta_z^- = -0.1$
	$\theta_z^0 = 0$
	$K = 0.14$

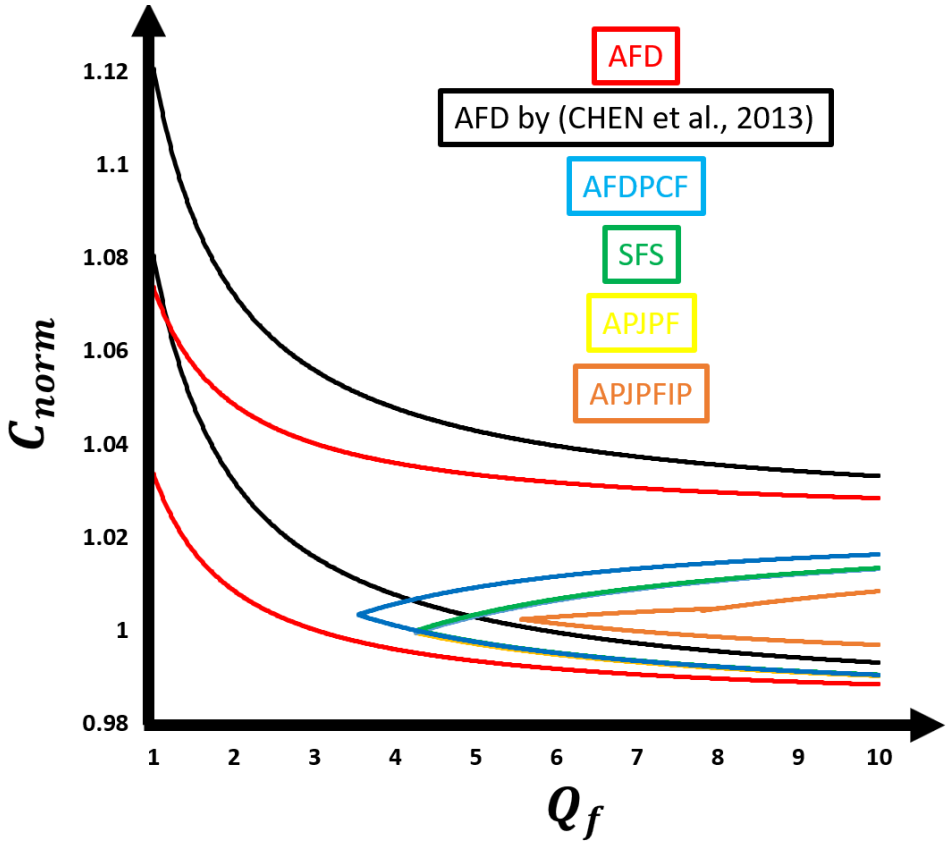
Source: Author.

4.6 Non-Detection Zone Comparison

In order to compare the performance of the analyzed strategies, Figure 4.4 maps the NDZ of each one in the $\boldsymbol{Q_f\ x\ C_{norm}}$ plan for the parameters described by Table 4.3. As can be seen, the fixed parametrized solutions (AFD and AFD by (CHEN et al., 2013)) present NDZ for all of the values of $\boldsymbol{Q_f}$. Futhermore, it is possible to state that they exhibit equivalent areas. However, it is also possible to notice that the AFD by (CHEN et al., 2013) NDZ is located in a

superior position if compared to the classic AFD scheme what, in turn, implies on the fact that the solutions tend to result in false negative islanding diagnoses for more capacitive loads, which are, in turn, rarer than inductive ones. The other methods can present reduced NDZ, since it was verified that this region does not existi for a range of quality factor values. The AFDPCF eradicates the NDZ for $\boldsymbol{Q_f = [0; 3.6]}$ and the SFS and the APJPF for $\boldsymbol{Q_f = [0; 4.1]}$. Finally, it is mandatory to highlight that the smallest NDZ is reached by the proposed method that eliminates the NDZ for $\boldsymbol{Q_f = [0; 5.56]}$.

Figure 4.4 – NDZ of each method for the parameters of Table 4.1.



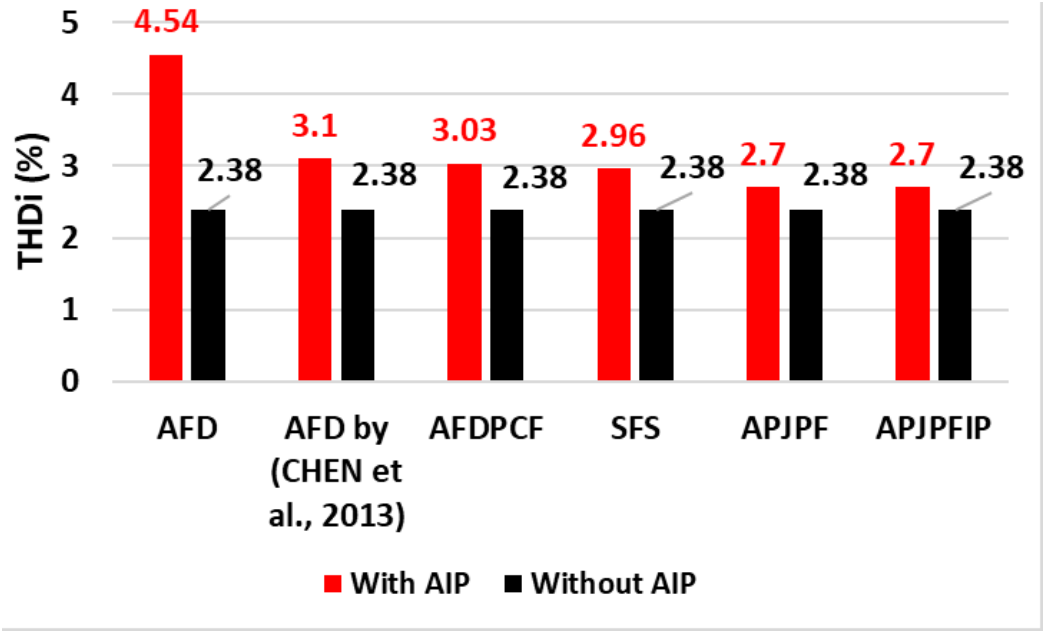
Source: Author.

4.7 Total Harmonic Distortion of Current Results

Operating under nominal conditions, the inverter described in Figure 4.1 shows a THDi rate of 2.38%. To compare the THDi demanded by each method for islanding detection, Figure 4.5 illustrates the harmonic content of the inverter's output current before and after the implementation of the active AIP strategy. As can be seen, the worst result was produced by the AFD algorithm, which increased the THDi rate from 2.38% to 4.54%. The methods AFD

by (CHEN et al., 2013), SFS, and AFDPCF yielded very similar results, with the harmonic distortion rate remaining around 3%. The best performance in this indicator was achieved by the APJPF and APJPFPI, both presenting the same THDi of 2.7%.

Figure 4.5 – THDi rate reached by each AIP method.



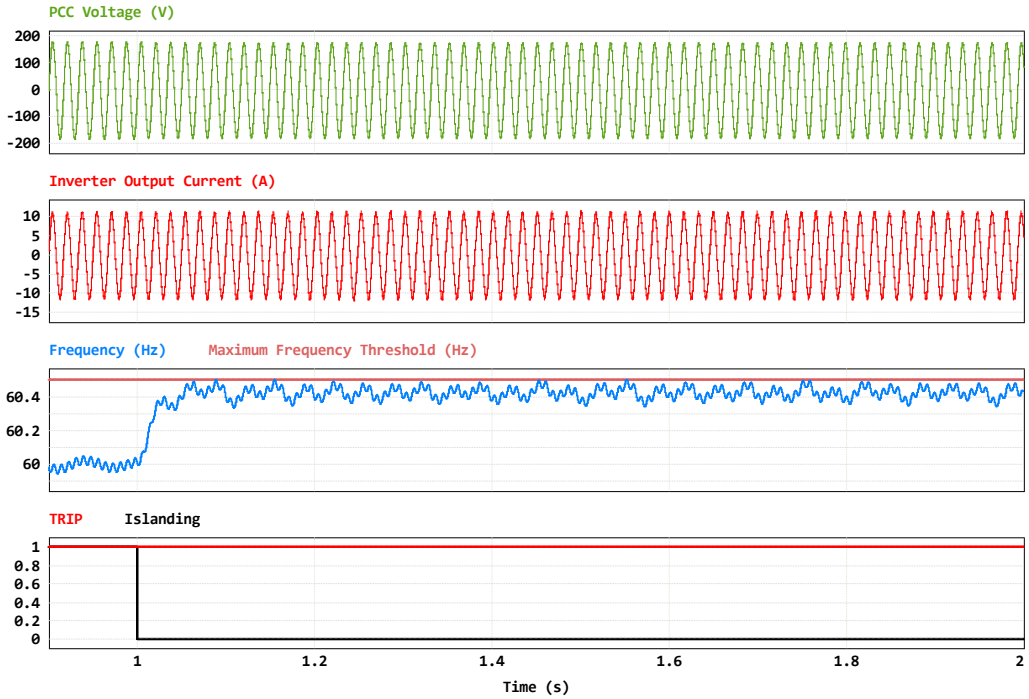
Source: Author.

4.8 Single Inverter Islanding Results: Detection Time

This section will cover the main results of detection time and THDi reached by each one of the analyzed strategies. It will be divided into 7 subsections, one for each of the six methods and, finally, the last subsection will cover the comparison of the results obtained for each strategy. Figures 4.6 and 4.7 illustrate the procedure of obtaining the total detection time.

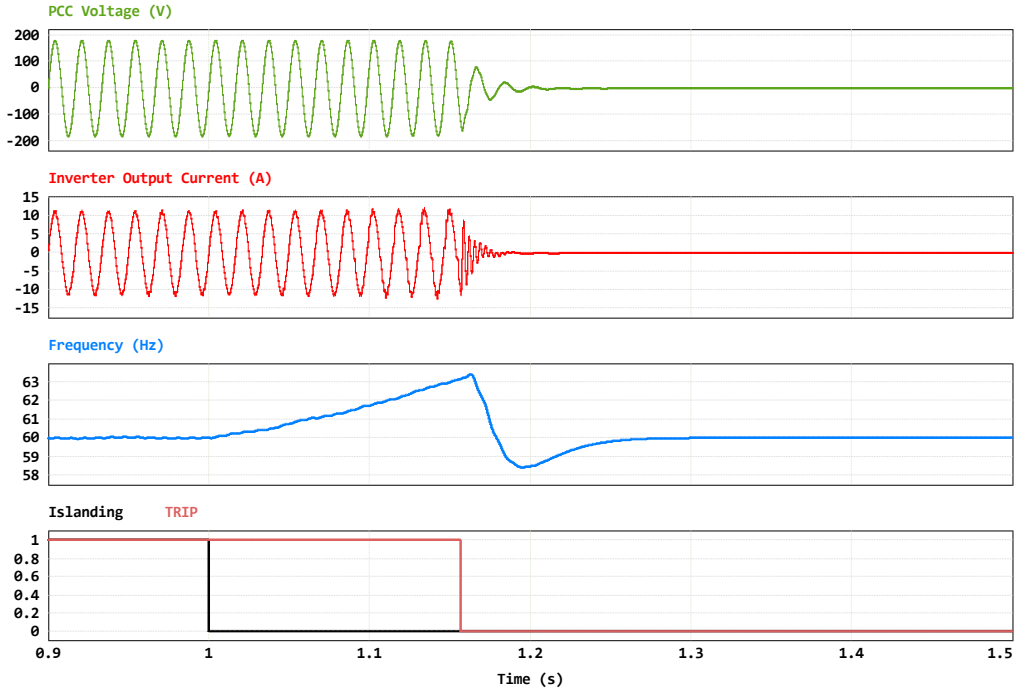
Figure 4.6 demonstrates the PCC voltage, the inverter output current after the adoption of the AFD algorithm, the values of frequency, the Islanding Signal (responsible for determining the grid interruption) and the TRIP signal (that marks the islanding detection). The value for quality factor was 2.5 and for normalized capacitance 1.01. This is one NDZ case, since the method was not able to detect the grid disconnection. Figure 4.7, on the other hand, displays the same electrical quantities for the APJPFIP method. The detection time was 114ms. An analogous procedure was adopted to find the other detection time results, so the graphical form of the other results will not be showed to avoid repetition.

Figure 4.6 – AFD detection time for a single inverter islanding.



Source: Author.

Figure 4.7 – APJPFIP detection time for a single inverter islanding.



Source: Author.

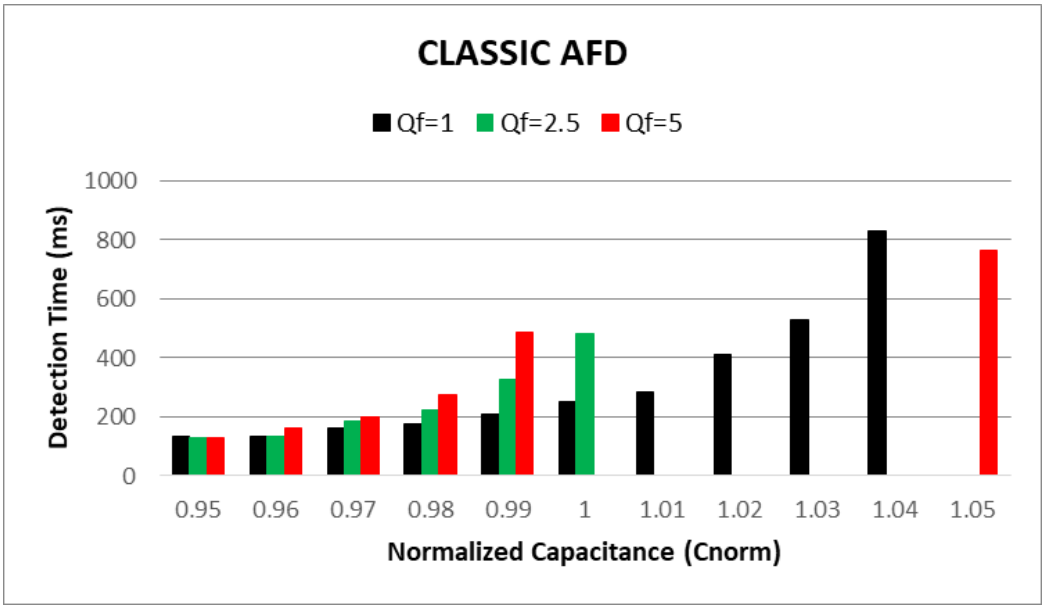
Figure 4.7, on the other hand, displays the same electrical quantities for the APJPFIP method. The detection time was 114ms. An analogous procedure was adopted to find the other

detection time results, so the graphical form of the other results will not be showed to avoid repetition. The following subsections will present graphs that summarize the detection time results for each of the adopted quality factors. For each normalized capacitance value, the detection times achieved by each method will be shown. If, for a given normalized capacitance value, the result for one of the methods is not displayed, it indicates that this method encountered a Non-Detection Zone (NDZ) case.

4.8.1 AFD single inverter islanding results.

Figure 4.8 presents the results of detection time reached by the Classic AFD algorithm for three different values of quality factor.

Figure 4.8 – AFD detection time for a single inverter islanding.



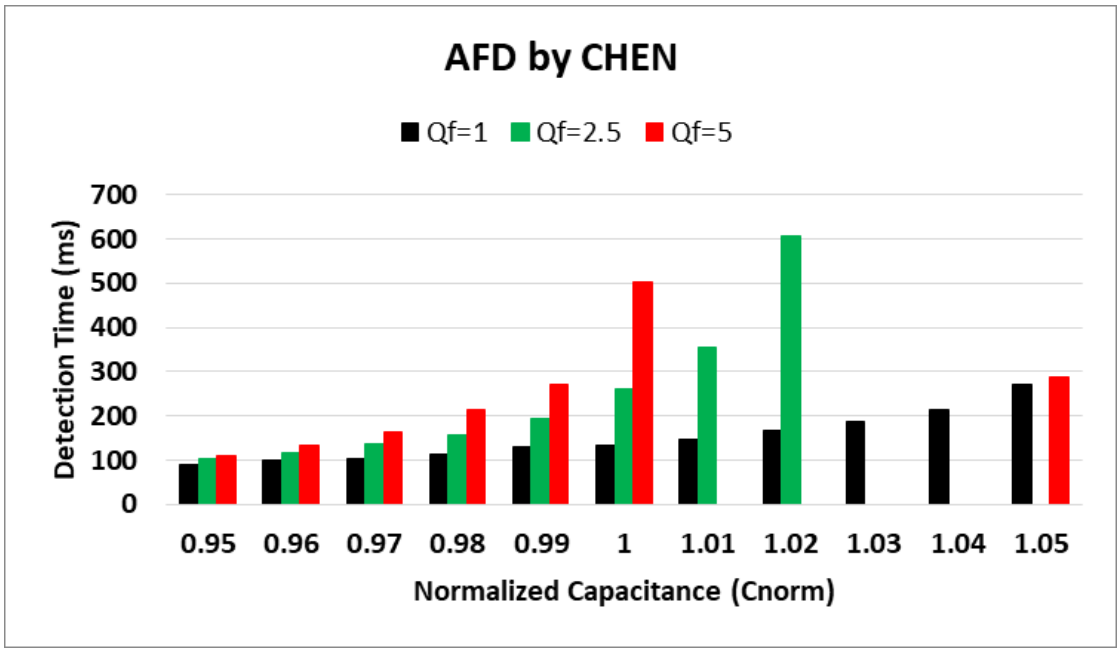
Source: Author.

As it is possible to notice, the AFD algorithm, as parametrized, has a good performance for more inductive load ($C_{norm} < 1$), however, its detection capability is highly affected by more capacitive loads. It is also important to highlight that the quality factor is a key variable in this analysis, since the growing of Q_f slows the islanding detection and increases the number of NDZ cases. In this sense, the algorithm has incurred NDZ for one case for $Q_f = 1$, four cases for $Q_f = 2.5$ and in five cases for $Q_f = 5$.

4.8.2 AFD by (Chen et. al, 2013) single inverter islanding results.

Figure 4.9 presents the results of detection time reached by the AFD by (Chen et. al, 2013) algorithm for three different values of quality factor. As it is possible to notice, the method shows better performance for more inductive loads, reaching fast islanding detection for all of the cases in which $C_{norm} < 1$. However, the detection time shows a tendency of growing with the increasing of the normalized capacitance and of the quality factor. In general, this scheme showed better performance when compared to the classic AFD, since it was able to detect the grid interruption for all the tests in which $Q_f = 1$ and presented less cases of NDZ: three cases for $Q_f = 2.5$ and four cases for $Q_f = 5$.

Figure 4.9 – AFD by (Chen et. al, 2013) detection time for a single inverter islanding.

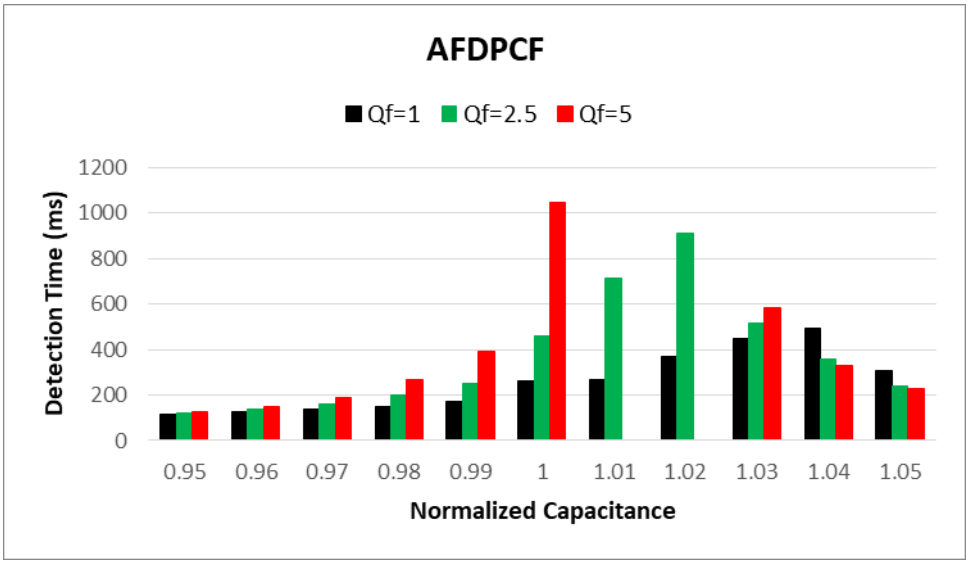


Source: Author.

4.8.3 AFDPCF single inverter islanding results

Figure 4.10 presents the results of detection time reached by the AFDPCF algorithm for three different values of quality factor. It is possible to notice that this strategy demands higher detection time in comparison with the two others AIP solution, even exceeding the 1s detection threshold for the condition $C_{norm} = 1$ and $Q_f = 5$. However, differently of the AFD and AFD by (CHEN el. al, 2013), the APFPCF was able of detecting the loss of mains for all the tested cases for $Q_f = 1$ and $Q_f = 2.5$, incurring in the NDZ for two cases for $Q_f = 5$.

Figure 4.10 – AFDPCF detection time for a single inverter islanding.

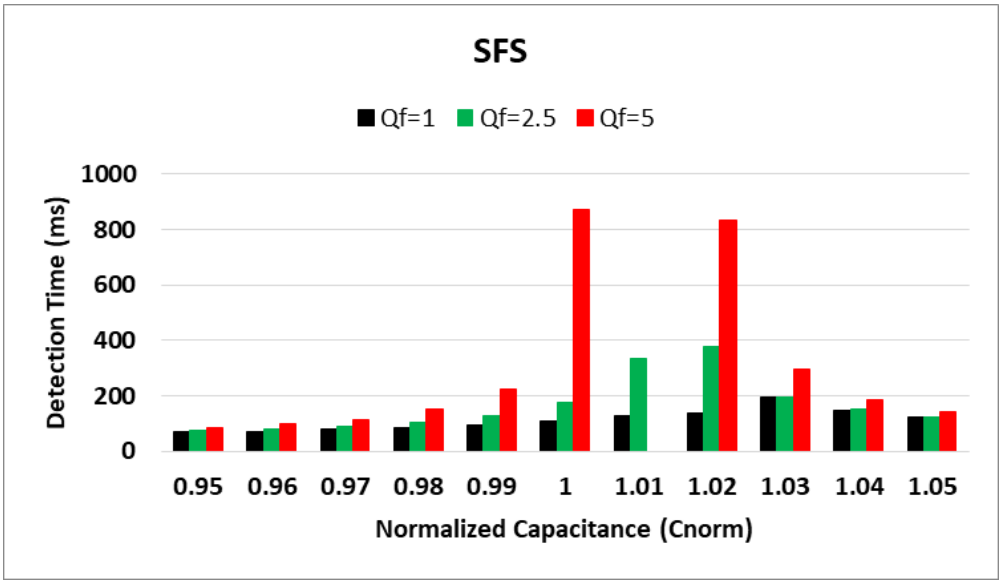


Source: Author.

4.8.4 SFS single inverter islanding results

Figure 4.11 presents the results of detection time reached by the SFS algorithm for three different values of quality factor.

Figure 4.11 – SFS detection time for a single inverter islanding.



Source: Author.

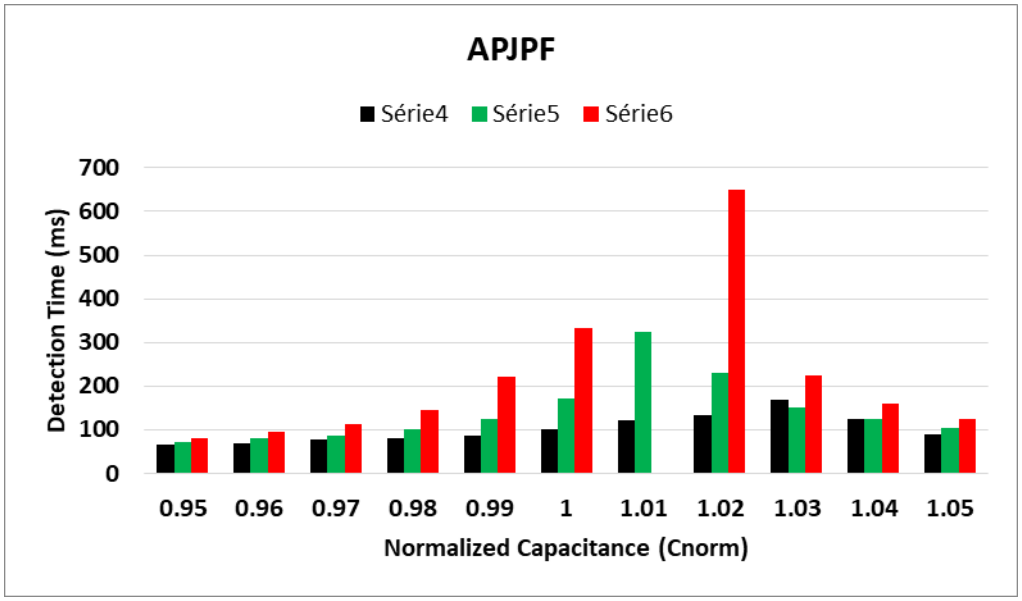
It is possible to notice that the SFS algorithm was able to perform the islanding detection to all of the 11 values of normalized capacitance for $Q_f = 1$ and $Q_f = 2.5$. Moreover, this method was able to reach the positive islanding diagnosis in less than 200ms for all of the C_{norm}

values for $Q_f = 1$, being the fastest, so far, for this condition. Additionally, the SFS reduced the NDZ cases in comparison with the other already tested solutions, incurring in non-detection only for the condition in which $Q_f = 5$ and $C_{norm} = 1.01$.

4.8.5 APJPF single inverter islanding results

Figure 4.12 presents the results of detection time reached by the APJPF algorithm for three different values of quality factor.

Figure 4.12 – SFS detection time for a single inverter islanding.



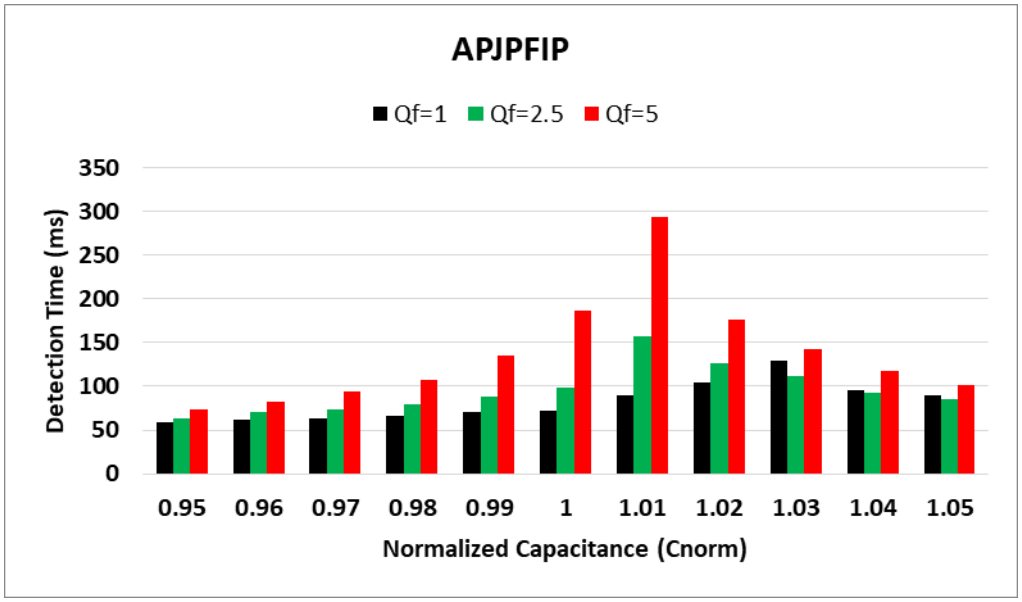
Source: Author.

It is possible to notice that the APJPF algorithm was able to detect islanding for all of the capacitance conditions for $Q_f = 1$ and $Q_f = 2.5$. Like the SFS algorithm, however, the method was unable to perform the grid interruption detection for the load condition in which $Q_f = 5$ and $C_{norm} = 1.01$. However, it is important to cite that the APJPF reached faster islanding detection than the SFS scheme for all of the performed tests as will be evidenced by subsection 4.6.7.

4.8.6 APJPFIP single inverter islanding results

Figure 4.13 presents the results of detection time reached by the APJPFIP algorithm for three different values of quality factor.

Figure 4.13 – APJPFIP detection time for a single inverter islanding.



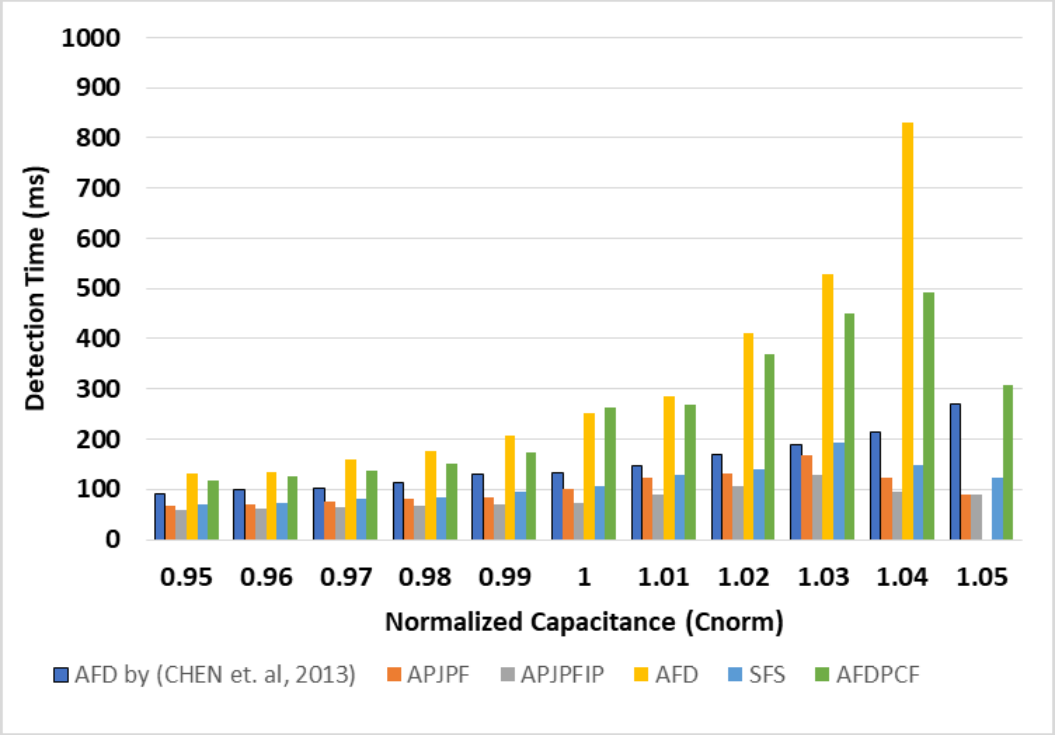
Source: Author.

It is possible to notice that this algorithm was able to perform the islanding detection for all load conditions, independently of Q_f and C_{norm}, being the only capable of performing the islanding diagnosis without occurring in NDZ cases. It accomplished the islanding detection in a lower detection time if compared to the other analyzed AIP, as will be explained by subsection 4.8.7.

4.8.7 Time Detection Comparison

It is mandatory to compare the results in the same graph, in order to attest the claimed reduction time by the adoption of the proposed solution. Figure 4.14 compares the detection time reached by each one of the compared strategies for $Q_f = 1$. In general, all of the methods performed fast and accurate islanding detection for more inductive loads. For more capacitive loads, on the other hand, it is possible to notice a tendency of the growing of the detection time for the AFD, for the AFDPCF and for the AFD by (CHEN et al., 2013). The only NDZ case was obtained by the classic AFD in $C_{norm} = 1.05$. Finally, it is important to state that for all of the tested conditions, the proposed APJPFIP accomplished the fastest detection, followed by the APJPF and for the SFS method.

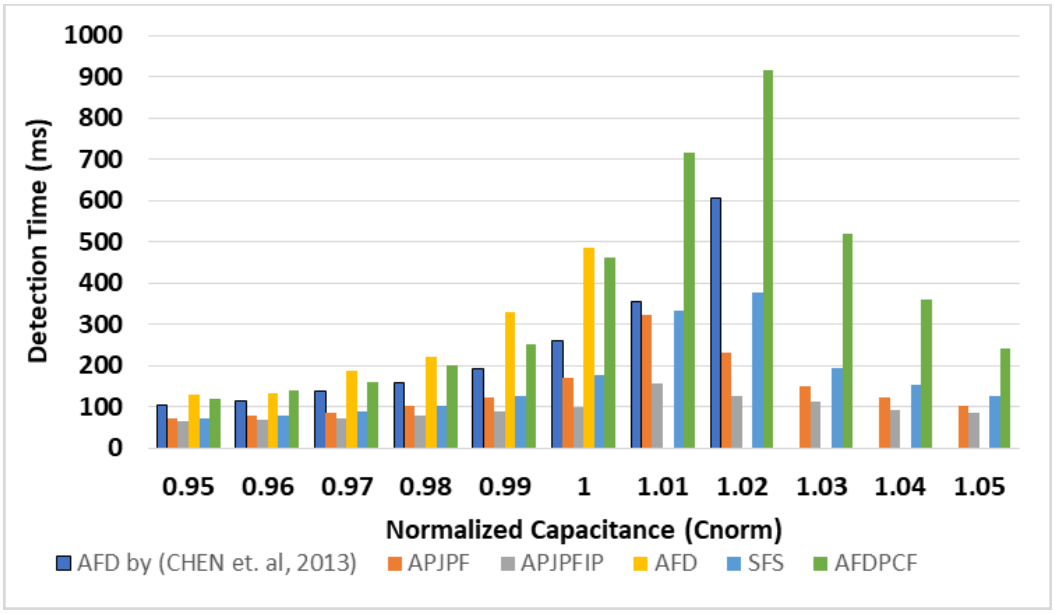
Figure 4.14 – Comparison of the detection time for $Q_f = 1$.



Source: Author.

Figure 4.15, on its hand, consists of the comparison of the reached detection times for the $Q_f = 2.5$ condition.

Figure 4.15 – Comparison of the detection time for $Q_f = 2.5$.

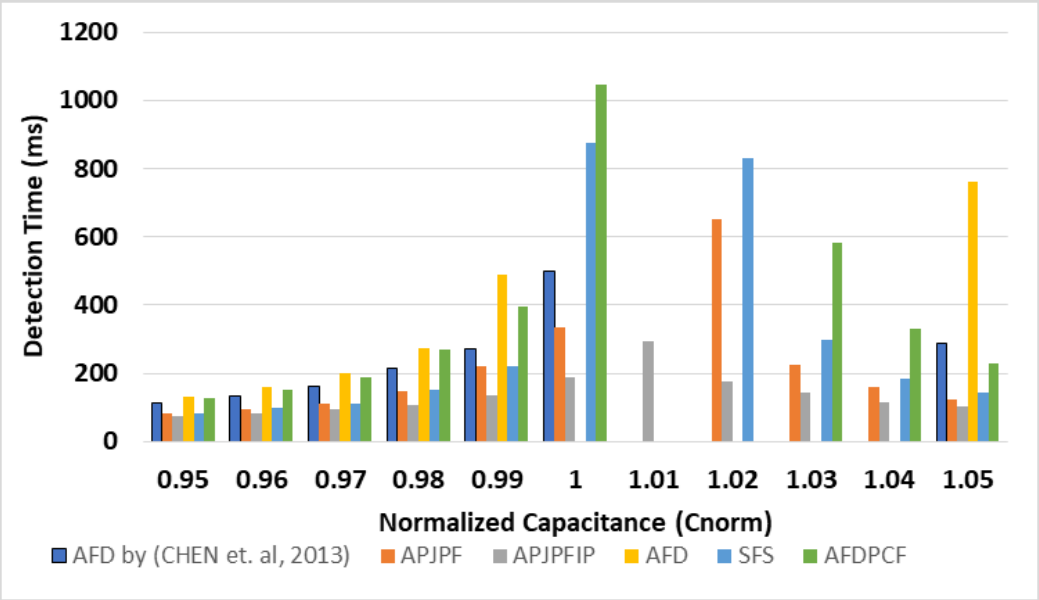


Source: Author.

It is possible to state that all methods accomplished fast islanding detection for more inductive loads. The methods with fixed parameterization, Classic AFD and AFD by (CHEN et al., 2013) incurred in, respectively, five and three NDZ cases. All of the other schemes reached accurate loss of mains detection for all of the values of C_{norm}. The proposed scheme accomplished lower detection time for all load conditions, followed, respectively, by the APJPF, SFS and AFDPCF.

Finally, Figure 4.16 shows the comparison of the reached detection times for the $Q_f = 5$ condition. As previously mentioned, this is an extremely adverse condition and therefore is not part of the considered standards recommendations. However, testing the AIP's in this hostile condition is a good indicator to attest the main performance differences among them. In this sense, the proposed APJPFIP was the only strategy capable of detecting the islanding occurrence for all of the tested cases, presenting a lower detection time in comparison with all of the other solutions. The AFD and the AFD by (CHEN et al., 2013) incurred in NDZ cases for five and four values of C_{norm} and the other solutions were not able to diagnosis the islanding phenomenon for the condition in which $Q_f = 5$ and $C_{norm} = 1.01$.

Figure 4.16 – Comparison of the detection time for $Q_f = 5$.



Source: Author.

In general, the obtained results can be summarized by:

- All of the methods reached fast islanding detection for more inductive loads;
- The methods with fixed parameterization incurred in more NDZ cases;

- It is verified a tendency of the growing of the detection time for the fixed parametrized algorithms;
- The proposed scheme accomplished fast islanding detection for all load conditions;
- The load condition in which $Q_f = 5$ and $C_{norm} = 1.01$ was the most adverse for the correct islanding detection;

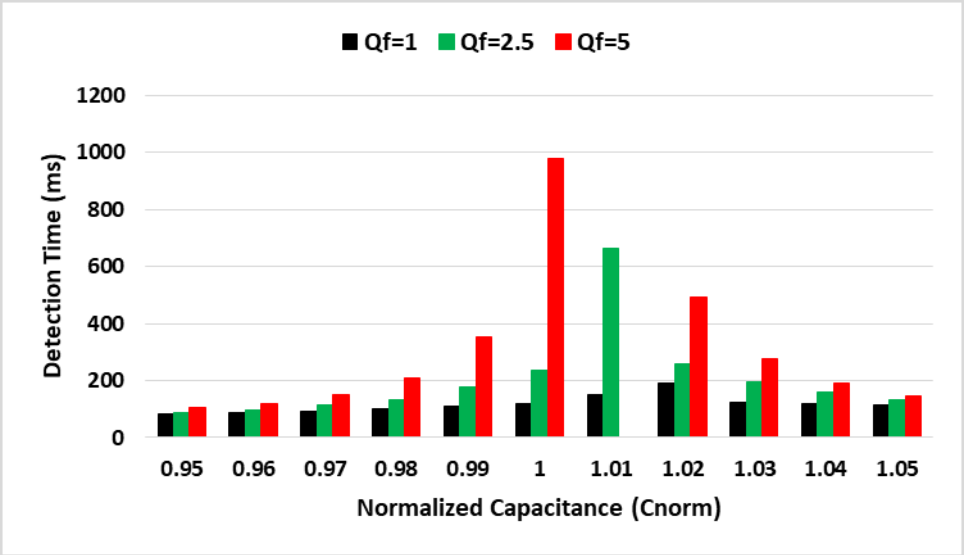
4.9 Double Inverter Islanding Results: Detection Time

This section aims to determine the performance of the analyzed AIP in a double inverter-based DGS system. The next subsections will show the detection time results obtained by the different combinations of the APJPFIP with the other AIP analyzed by this work. In total, each combination will be tested under three different quality factors values (presented in Table 4.2) and for a range of normalized capacitances that varies from 0.95 to 1.05, with a 0.01 increment. The upcoming subsections will display graphs that consolidate the detection time results for each quality factor used. For each normalized capacitance value, the detection times recorded by each method will be presented. If a combination's result is absent for a particular normalized capacitance value, this indicates that the method encountered a Non-Detection Zone (NDZ).

4.9.1 APJPFIP+AFD Combination.

Figure 4.17 shows the results of detection time reached by a combination of two inverters working, respectively, with the APJPFIP and with the Classic AFD for three different values of quality factor. As it is possible to notice, the combination of the two algorithms is able to detect the grid interruption for all the tested cases for $\boldsymbol{Q_f = 1}$ and $\boldsymbol{Q_f = 2.5}$ and the only NDZ case happened for $\boldsymbol{Q_f = 5}$ and $\boldsymbol{C_{nor} = 1.01}$.

Figure 4.17 – Time detection results for the APJPFIP+AFD Combination.

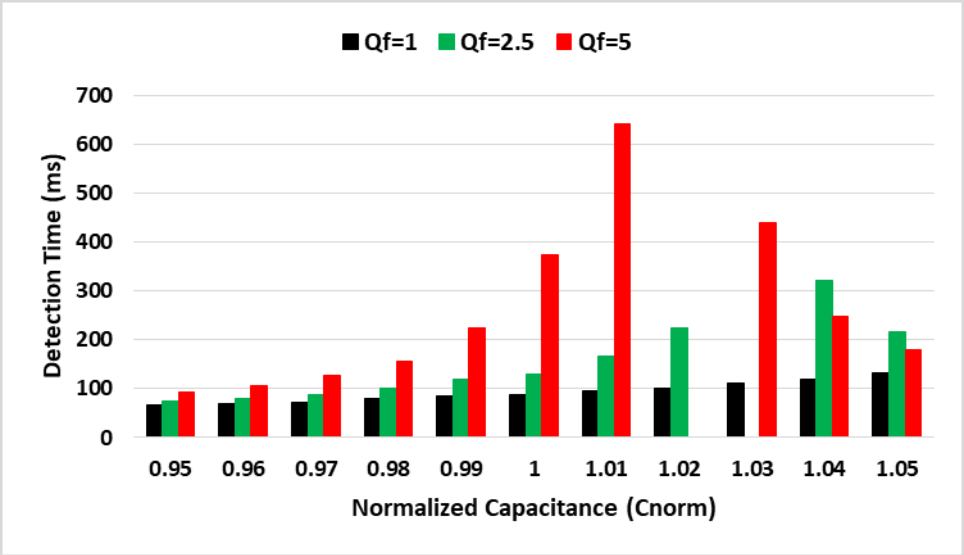


Source: Author.

4.9.2 APJPFIP+AFD by (CHEN et al., 2013) Combination.

Figure 4.18 shows the results of detection time reached by a combination of two inverters working, respectively, with the APJPFIP and with the AFD by (CHEN et al., 2013) for three different values of quality factor. As it is possible to notice, the combination of the two algorithms is able to detect the grid interruption for all the tested cases for $\boldsymbol{Q_f = 1}$. Although this combination was faster than the previous one for the detectable conditions, it incurred in two NDZ cases for $\boldsymbol{Q_f = 2.5}$ and $\boldsymbol{C_{nor} = 1.03}$ and for $\boldsymbol{Q_f = 5}$ and $\boldsymbol{C_{nor} = 1.02}$, respectively.

Figure 4.18 – Time detection results for the APJPFIP+AFD by (CHEN et al., 2013) combination.

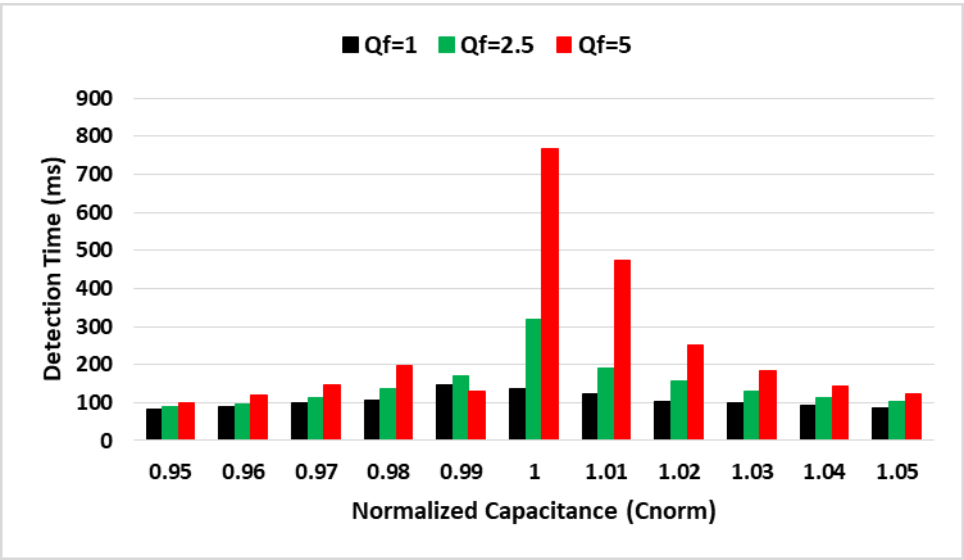


Source: Author.

4.9.3 APJPFIP+AFDPCF Combination.

Figure 4.19 shows the results of detection time reached by a combination of two inverters working, respectively, with the APJPFIP and the AFDPCF for three different values of quality factor.

Figure 4.19 - Time detection results for the APJPFIP+AFDPCF combination.



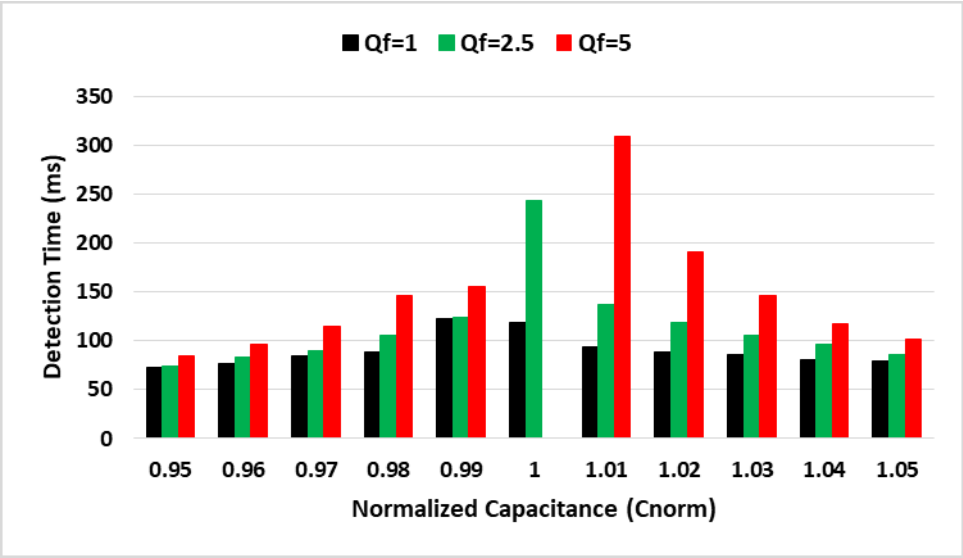
Source: Author.

As it is possible to notice, the combination of the two algorithms is able to detect the grid interruption for all the load conditions. In general, the equilibrium condition, where $\boldsymbol{C_{norm} = 1}$, was the most adverse for detecting islanding, since this was the condition with the longest detection time for all of the $\boldsymbol{Q_f}$ values. No significant difference was observed for more inductive or for more capacitive loads, fact that demostrate the capability of following the frequency drift imposed by the local load.

4.9.4 APJPFIP+SFS Combination.

Figure 4.20 shows the results of detection time reached by a combination of two inverters working, respectively, with the APJPFIP and with the SFS for three different values of quality factor. As it is possible to notice, the combination of the two algorithms is able to detect the grid interruption for all the load conditions, except for $\boldsymbol{Q_f = 5}$ and $\boldsymbol{C_{norm} = 1}$. It is important, however, to highlight that, for all of the detected cases, this combination was faster than the previous one.

Figure 4.20 – Time detection results for the APJPFIP+SFS combination.



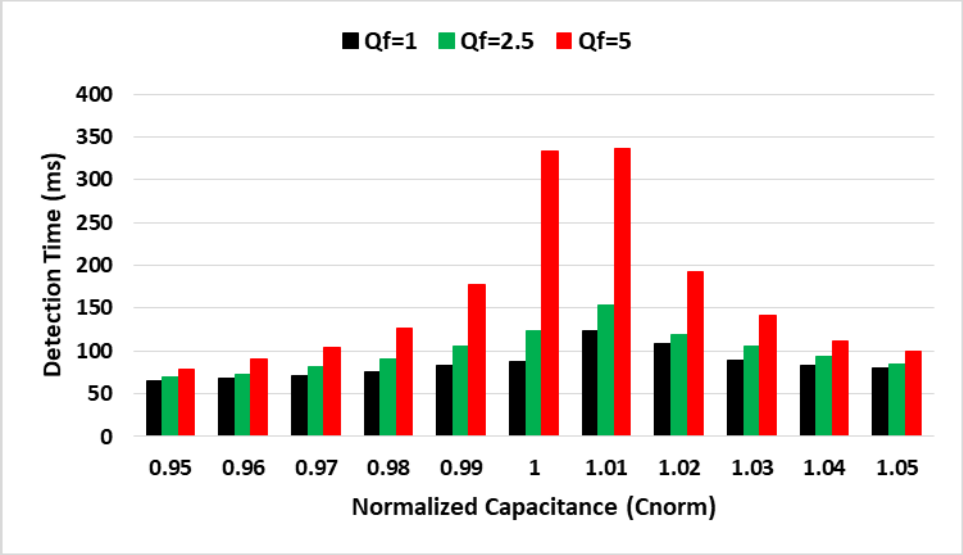
Source: Author.

4.9.5 APJPFIP+APJPF Combination.

Figure 4.21 shows the results of detection time reached by a combination of two inverters working, respectively, with the APJPFIP and with the APJPF for three different values of quality factor. This combination was able to accomplished successful islanding detection for

all of the tested cases. It is possible to highlight that the detection time remained below of 200ms for all load conditions, except for $\boldsymbol{Q_f = 5}$ and $\boldsymbol{C_{norm} = [1; 101]}$.

Figure 4.21 – Time detection results for the APJPFIP+APJPF combination.

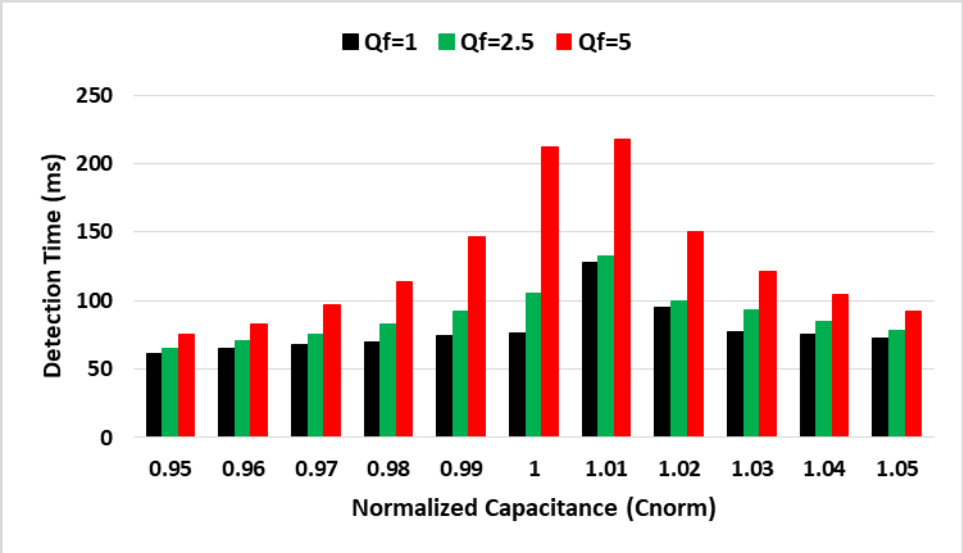


Source: Author.

4.9.6 APJPFIP+APJPFIP Combination.

Figure 4.22 shows the results of detection time reached by a combination of two inverters working with the proposed solution for three different values of quality factor.

Figure 4.22 – Time detection results for the APJPFIP+APJPFIP combination.



Source: Author.

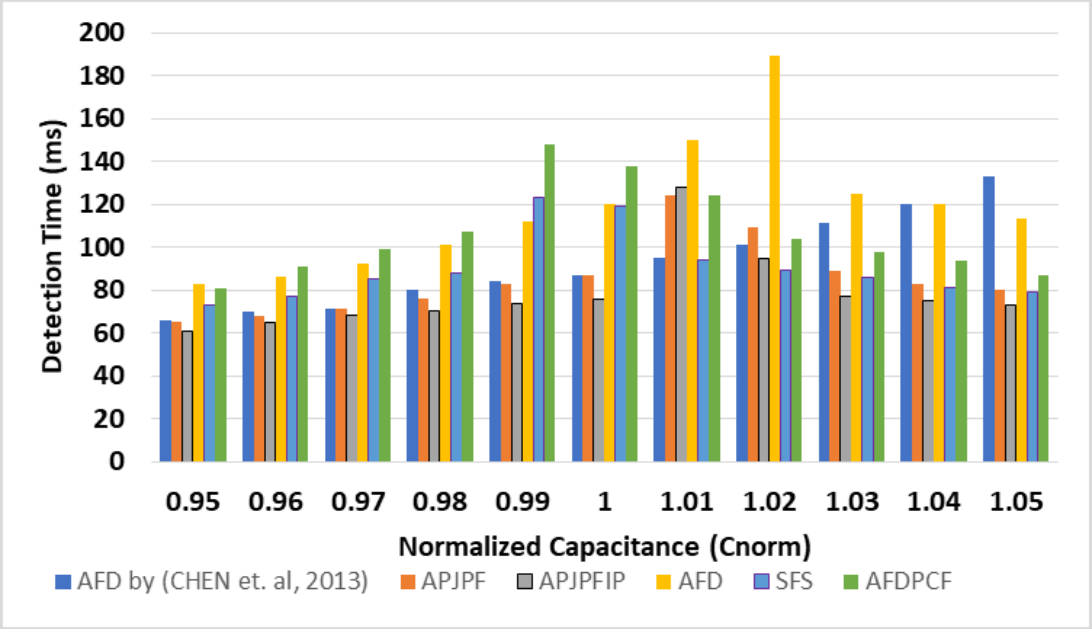
This combination was able to accomplished successful islanding detection for all of the tested cases. It is possible to highlight that the detection time remained below of 150ms for all load conditions, except for $\boldsymbol{Q_f = 5}$ and $\boldsymbol{C_{norm}} = [\mathbf{1}; \mathbf{101}]$. Finally, it is also necessary to highlight that this combination reached faster islanding detection for all load conditions as will be shown in the next subsection.

4.9.7 Time Detection Comparison.

Figure 4.23 compares the detection time reached by each one of the analyzed combinations for $Q_f = 1$. In general, all of the combinations performed fast and accurate islanding detection for all load conditions and the obtained detection time results were not influenced by the local load characteristic. Thus, the islanding detection was accomplished in less than 200 ms for all of the tested cases and no NDZ case was observed. The APJPFIP+ APJPFIP combination reached the fastest detection for all the experiments, followed by the APJPFIP+APJPF and for the APJPFIP+SFS combination. Figure 4.24 compare the detection time reached by each one of the analyzed combinations for $Q_f = 2.5$. As it can be seen, the only NDZ case was obtained by the APJPFIP+AFD by (CHEN et al., 2013) for the load condition in which $C_{norm} = 1.03$. For all of the detected cases, the APJPFIP+ APJPFIP combination reached the fastest detection, followed by the APJPFIP+APJPF and for the APJPFIP+SFS combination. The APJPFPI+AFD combination, on the other hand, were the slower for all load conditions and the results indicate a time dependence on the load characteristic once the detection for more capacitive loads was slower than for more inductive loads.

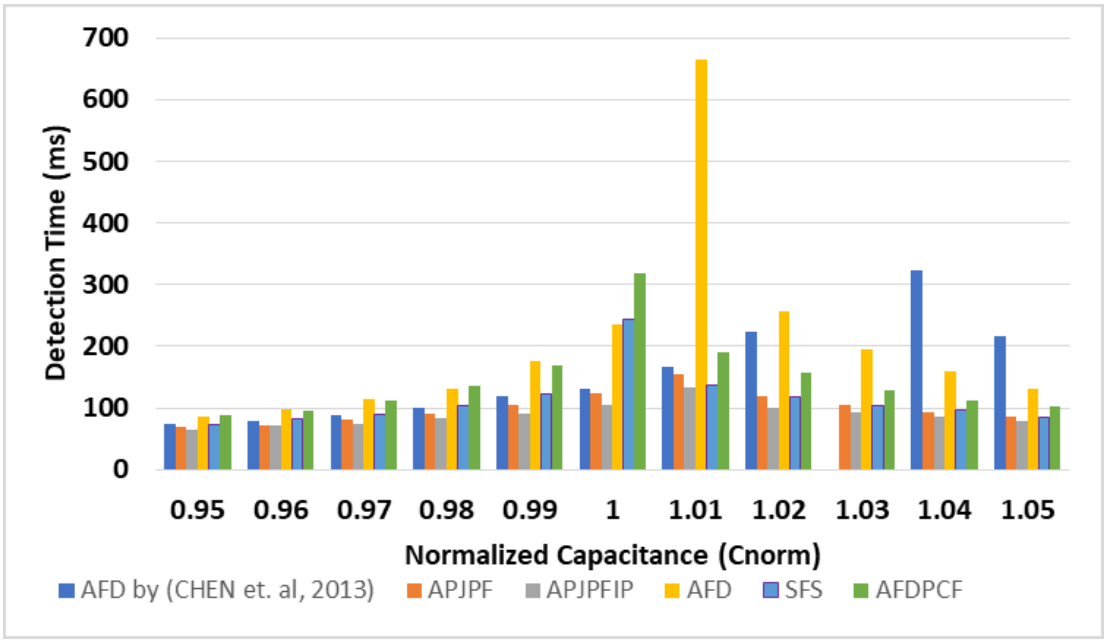
Figure 4.25 compare the detection time reached by each one of the analyzed combinations for $Q_f = 5$. As it can be seen, it was obtained three NDZ cases. The APJPFIP+AFD combination did not detect the islanding for $C_{norm} = 1.01$, the APJPFIP+SFS combination failed for $C_{norm} = 1$ and the APJPFIP+AFD by (CHEN et al., 2013) combination for $C_{norm} = 1.02$. For all of the detected cases, the APJPFIP+ APJPFIP combination reached the fastest detection, followed by the APJPFIP+APJPF and for the APJPFIP+AFDPCF combination. The APJPFPI+AFD combination, on the other hand, reached the worst results for all load conditions and presented a time dependence on the load characteristic, since the detection for more capacitive loads was slower than for more inductive loads. A similar load dependency was verified for the APJPFIP+AFD by (CHEN et al., 2013) combination.

Figure 4.23 – Comparison of the detection time for $Q_f = 1$.



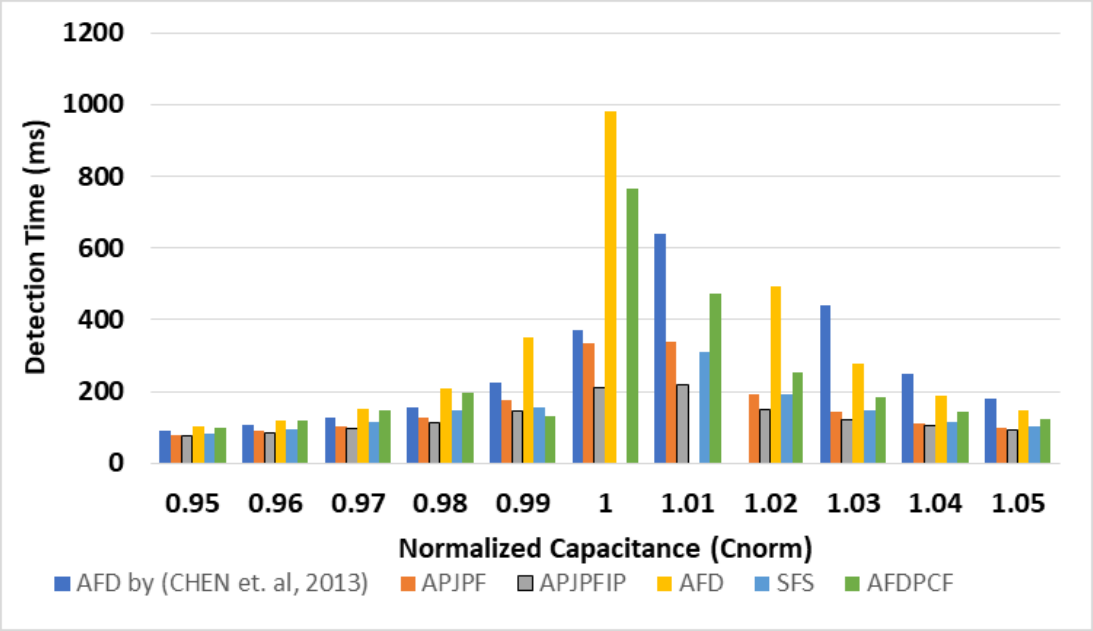
Source: Author.

Figure 4.24 – Comparison of the detection time for $Q_f = 2.5$.



Source: Author.

Figure 4.25 – Comparison of the detection time for $\boldsymbol{Q_f = 5}$.



Source: Author.

In general, the obtained results can be summarized by:

- All of the combinations showed good performance for unitary quality factor loads;
- The combinations with fixed parametrized algorithms incurred in more NDZ cases;
- It is verified a tendency of the growing of the detection time for the combinations with fixed parametrized algorithms for more capacitive loads, especially for high quality factor.
- The APJPFIP+APJPFIP combination accomplished fast detection for all of the tested cases.
- The presence of the APJPFIP improves the detection capabilities of the other strategies. Consequently, the combination APJPFIP+AFD, for instance, incurred in less NDZ cases than the AFD algorithm when working in a single-inverter DGS.

4.10 Final Considerations

This chapter discussed the potential of the proposed strategy in comparison to other well-known AIP solutions: AFD, AFD by Chen et al. (2013), AFDPCF, SFS, and APJPF. The inverter power and control structure were presented, highlighting the adopted PLL and the passive anti-islanding solution. The active methods were compared based on three key performance indicators: NDZ, THDi, and detection time.

Concerning NDZ, it was possible to conclude that exists two groups of methods. The first group is formed by the strategies with fixed parameterization. Those methods present a complete NDZ and, therefore, for all values of Q_f, there is an interval of C_{norm} for which the solution is unable to detect the loss of mains. The other group, on the other hand, present variable parameters and can eliminate the NDZ for a given range of Q_f. As demonstrated, the AFDPCF eradicates the NDZ for $Q_f = [0; 3.6]$, the SFS and the APJPF for $Q_f = [0; 4.1]$ and the proposed APJPFIP for $Q_f = [0; 5.56]$, accomplishing the smaller NDZ among the compared AIP solutions.

Regarding THDi, the Classic AFD reached the worst qualitative result, demanding a 4.58% rate of harmonic content to perform the islanding detection. The methods AFD by (CHEN et al., 2013), SFS and the AFDPCF obtained very similar results in which the harmonic distortion rate remained around 3% and the APJPF and APJPFIP accomplished the lower TDHi result, totaling 2.7%. This fact, on its hand, shows the advantages of the intermittent perturbation of the θ_{Z_o} parameter that improves the islanding detection capabilities without the increasing of the harmonic content of the inverter output current.

In terms of detection time, the methods were tested in two different environments. In the first scenario, all methods were tested in a single-inverter DGS during an islanding event for a combination of three quality factor values and eleven normalized capacitance values, totaling 33 tests for each method. The results showed the superior performance of the proposed APJPFIP, which was the only strategy capable of detecting grid disconnection under all tested load conditions.

In the second scenario, the ability of the methods to detect islanding in a dual-inverter DGS setup was tested, with the APJPFIP combined with the other solutions. The local load was also parameterized according to the standards' recommendations, and the combinations were subjected to the same load conditions as in the previous tests. The results confirmed the efficiency of the APJPFIP method even in a multi-inverter DGS. Overall, the best result was obtained with the APJPFIP+APJPFIP combination.

CHAPTER V

Experimental Analysis Using Controller Hardware-in-the-Loop Setup

5.1 Introduction

The main goal of this chapter is to present the real-time implementation results to ensure the effectiveness of the proposed AIP technique. The tools used were: Typhoon® Hardware-in-the-Loop, Typhoon® Control Center, Texas Instruments LAUNCHXL-F28379D Development Kit, and Code Composer Studio. It is important to note that HIL technology is defined as the application of a Hardware-in-Test (HIT) system to enable real-time simulations. Depending on the specifications, application, and HIT, different test configurations can be used: Model-in-Loop (MIL), Software-in-Loop (SIL), Controller Hardware-in-the-Loop (C-HIL), and Power Hardware-in-the-Loop (P-HIL).

In a C-HIL setup, real-time simulation models a system, and an external Control Unit (HIT) interacts with it. The Control Unit is usually a microcontroller, a digital signal controller, or a digital signal processor. The connection between the real-time simulation and the Control Unit can be direct or use an interface board, depending on whether their input and output terminals are voltage-compatible. The real-time simulation generates waveforms representing the system's behavior, which the Control Unit processes using its control algorithm before sending control signals back to the simulation.

The use of C-HIL technology is justified because it allows testing physical power electronic devices in real-time without prototyping. The process of testing and validating islanding protection devices depends on strict parameterization of the load, which needs adjustment for different values of normalized capacitance. Therefore, using a HIL device reduces resource use and increases the accuracy of AIP algorithm evaluation.

The results will be divided into two subsections. The first will focus on a single-inverter environment. In this scenario, 792 tests were performed to compare the proposed technique's performance with other well-known strategies from the literature. The second subsection analyzes the strategy's performance in a multi-inverter islanded system. The first set of tests examines the proposed method's performance in parallel with other AIP strategies. The second

set tests the algorithm in a system with three inverters, and the third evaluates its performance in a system with four inverters.

5.2 Real Time Setup

Figure 5.1 shows the experimental setup used, consisting of the Typhoon HIL 404 equipment.

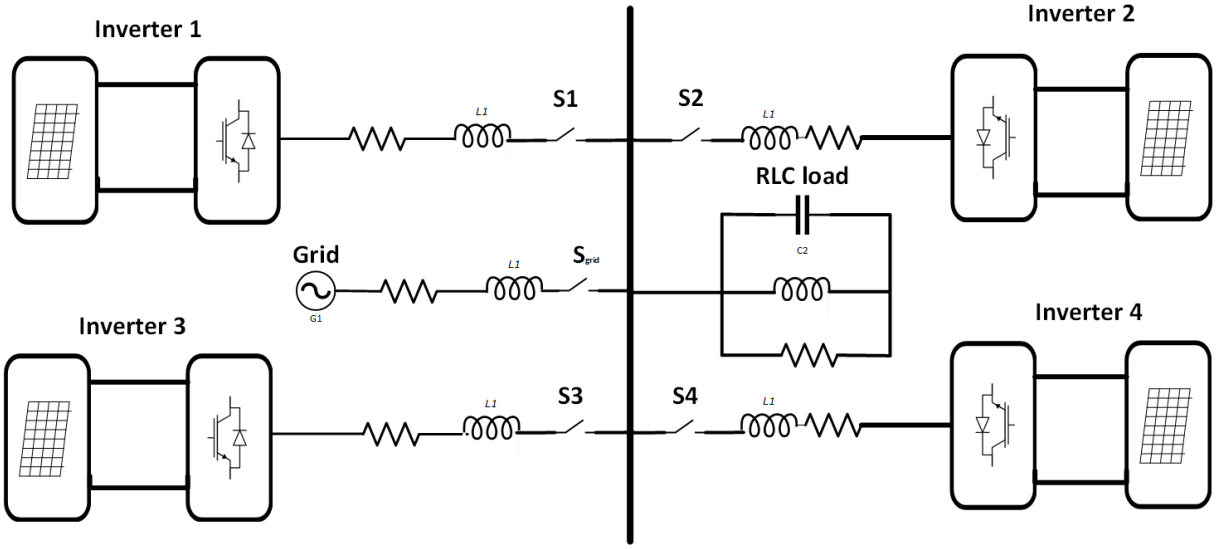
Figure 5.1 – Experimental Setup.

Source: Author.

5.3 System Description

The adopted system will be composed by four inverters connected to the grid as illustrated by Figure 5.2.

Figure 5.2 – Block diagram of the system.



Source: Author.

Each inverter will supply 25% of the active power demanded by the load when all four inverters are operating. When only three inverters are operating, the load will be adjusted to match the power output, with each inverter supplying 33% of the total power. Similar adjustments will be made for two and one-inverter scenarios. All distributed generation units are connected to the utility grid, and all interconnection impedances between the inverters and the grid are considered in the schematics. The load presents variable parameters and will be designed according to standards' recommendations.

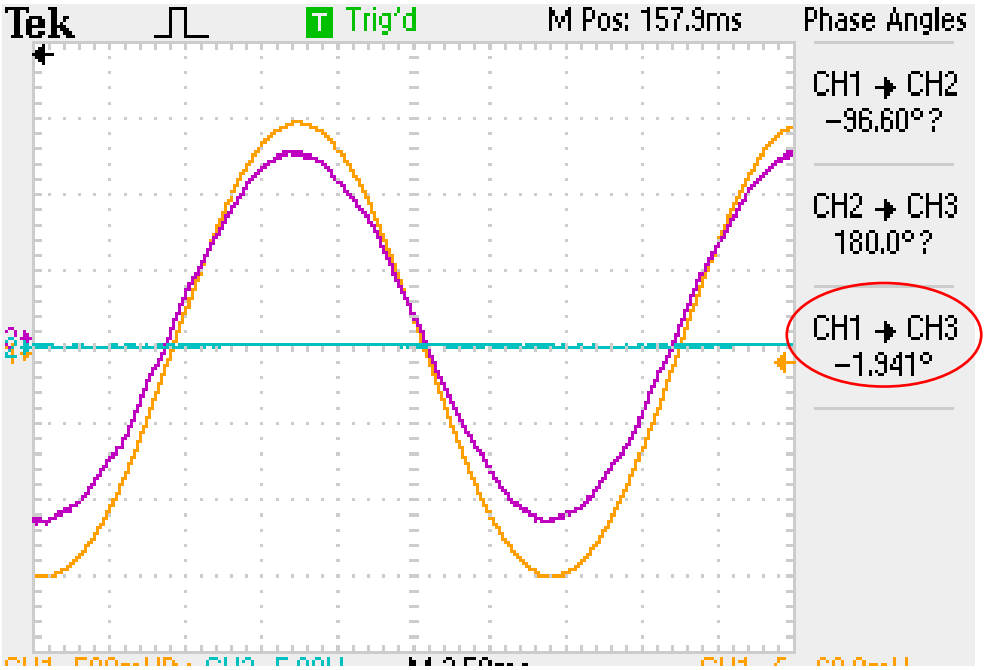
5.4 Methods Implementation

As extensively discussed in previous sections, active AIP methods can reduce the NDZ, thereby improving the security and reliability of the protection system. However, their adoption is linked to an increase in power quality intrusion. Figures 5.4, 5.5, and 5.6 present the inverter current results, PCC voltage, and grid current with the inverter connected to the grid and the RLC load described above. The load's normalized capacitance was maintained at Cnorm = 1. The purpose of these figures is to demonstrate the voltage-current synchronization of the inverter equipment, as well as to show the characteristic of the grid's current contribution.

Figure 5.4 shows the inverter operating without an islanding detection method. As observed, the inverter's power factor, without any anti-islanding method, is nearly unity.

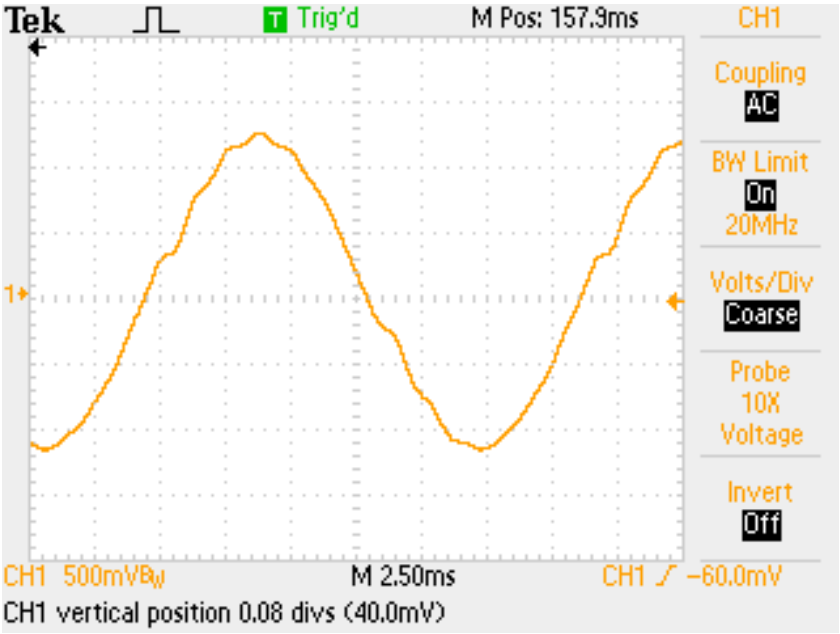
Measurements performed with a TEKTRONIX TPS 2024 oscilloscope showed a phase difference between current and voltage of -1.89 degrees, resulting in a power factor of 0.9994, proving the efficiency of the implemented SOGI PLL. Figures 5.3 to 5.9 show the inverter output current after each active AIP method implementation.

Figure 5.3 – Comparison between the waveforms of voltage and current before active AIP implementation.



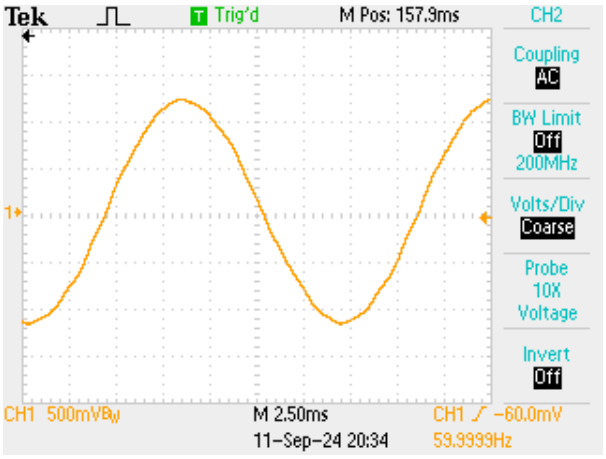
Source: Author.

Figure 5.4 – AFD current waveform.



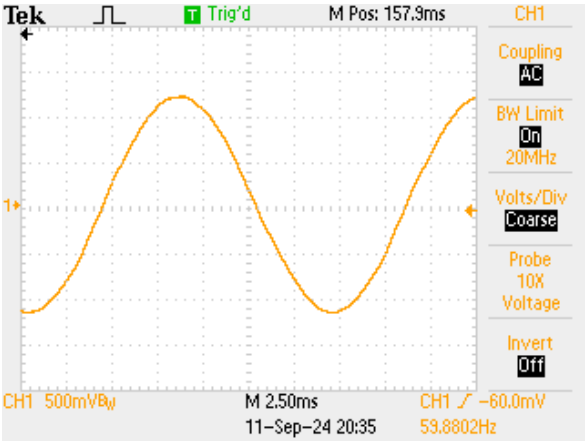
Source: Author.

Figure 5.5 – SFS current waveform.



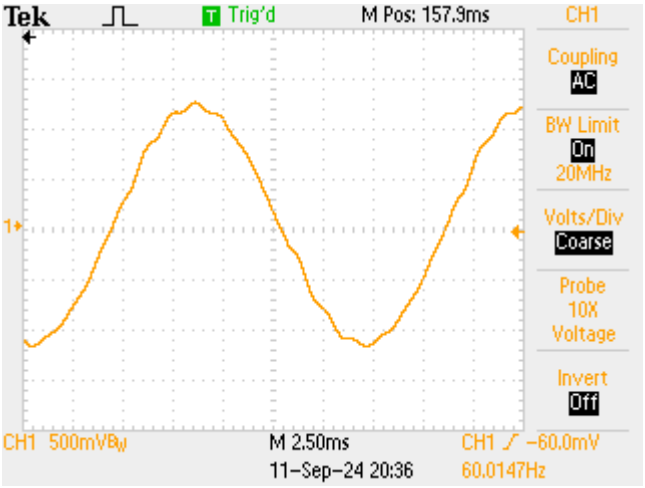
Source: Author.

Figure 5.6 – AFDPCF current waveform.



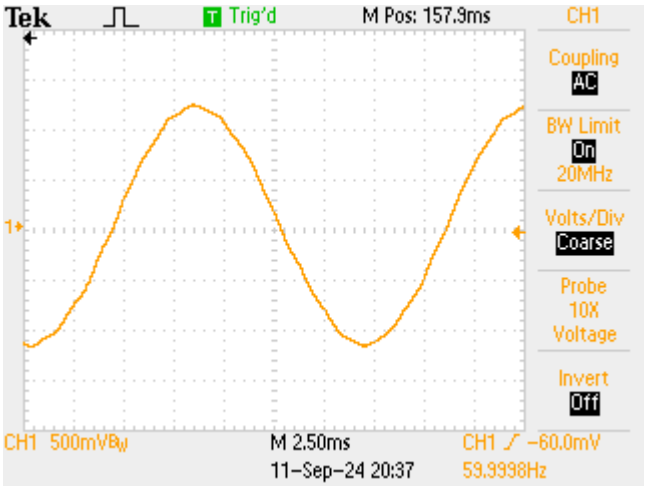
Source: Author.

Figure 5.7 – AFD by (CHEN et al., 2013) current waveform.



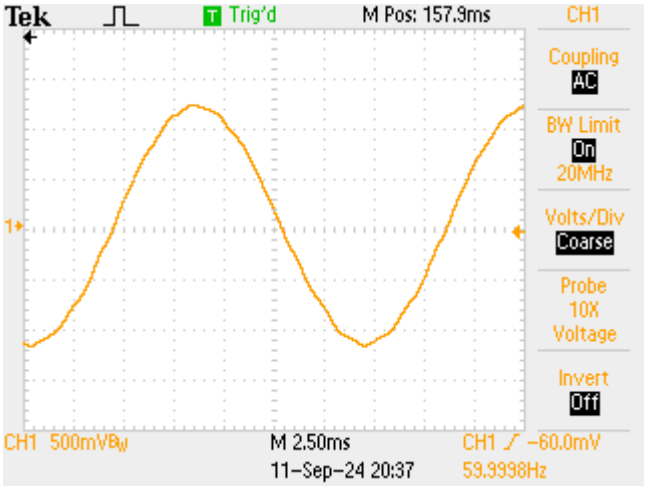
Source: Author.

Figure 5.8 – APJPF current waveform.



Source: Author.

Figure 5.9 – APJPFIP current waveform..



Source: Author.

5.5 Methodology

As previously mentioned, this work aims to compare the proposed anti-islanding technique with several well-established methods found in the literature: AFD, AFD by Chen et al. (2013), SFS, AFDPCF, and APJPF. During the methodology section for simulation results, it was explained the adopted values for quality factor, normalized capacitance and the tests would be performed. It also explained the key parameter index to evaluate the operation of the analyzed AIP methods: NDZ, detection time and THDi.

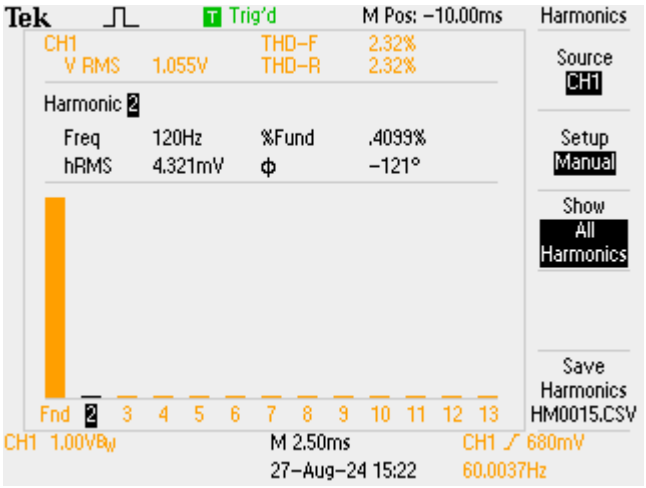
Regarding NDZ, it is important to note that it is a theoretical indicator and will not be discussed again in this subsection. However, the other two indicators must be obtained in a real-time implementation to validate the simulation results, considering the inherent non-idealities of the electrical system. THDi will be measured before and after the implementation of each method. As for detection time, this chapter will compare the performance of the implemented strategies and evaluate the proposed solution's capability to operate in parallel with other methods. This capability is essential for the successful integration of DGS and microgrids into the electrical system. Islanding detection is crucial for inverter manufacturing as it ensures the safe disconnection of inverters during grid disturbances, protecting equipment and personnel. In microgrids, effective islanding detection enhances system stability by preventing unintended power isolation and ensuring reliable, synchronized operation with the main grid.

5.6 THDi Analysis

As extensively discussed in previous sections, active AIP methods can reduce the NDZ, thereby improving the security and reliability of the protection system. However, their adoption is linked to an increase in the THDi rate. THDi is a qualitative indicator for renewable resources connected to the grid. The standards mentioned in this text establish maximum total and individual thresholds for current harmonic content. However, it is important to highlight that improving the power quality of commercial inverters up to these maximum thresholds and merely meeting Standards' recommendations is not enough to guarantee the best performance of a power electronic device. In light of the foregoing, this section will analyze how each method—including the proposed one—impacts the harmonic distortion of the inverter output current.

Firstly, it is important to know the inverter's THDi without active AIP. Figure 5.10 demonstrates the total harmonic content of the inverter output current obtained via Fast Fourier Transform (FFT) using a TEKTRONIX TPS2024B oscilloscope, which resulted in 2.32% harmonic distortion. Figure 5.4, in turn, demonstrates the harmonic orders of the inverter output current in comparison with the recommendations of the IEEE 929-2001 standard, proving conformity with each individual threshold. It is important to highlight that this result was found before any active AIP implementation. An analogous procedure was adopted to find the THDi after each analyzed methods was implemented.

Figure 5.10 – Harmonic content of the output inverter current with no active AIP.

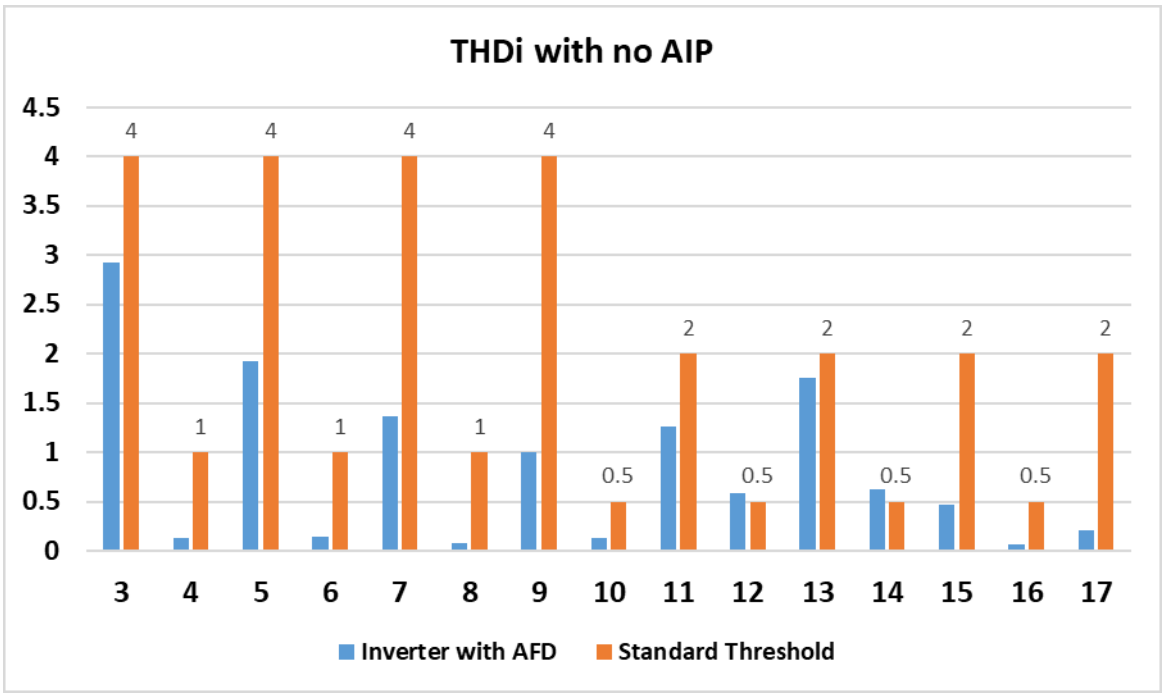


Source: Author.

In the context of modern DGS and hibrid microgrids, THDi is a very important qualitative parameter to ensure the correct electrical feeding of loads and to allow power flow from the generation plant to the main grid. In the view of the foregoing, more than just targeting the thresholds of the Standards, AIP research must focus on producing less disturbing active AIP methods to make inverter devices and, therefore, microgrids and DGS less polluting for the electrical system as a whole. Considering this, it is important to state that the proposed method reached the best qualitative result, totaling2.41%. The Classic AFD demonstrated the poorest qualitative performance, increasing THDi from 2.32% to 4.93%, nearing the threshold set by power quality standards. The harmonic content produced by AFDPCF was 3.01%, making it the second worst performer. The SFS algorithm recorded 2.85%, while both AFDPCF and APJPF achieved 2.5%. The best THDi result, therefore, was obtained by the proposed method, highlighting the benefits of intermittent perturbation of the θ_{Z_o} parameter, which enhances islanding detection capabilities without increasing the inverter's output current harmonic content.

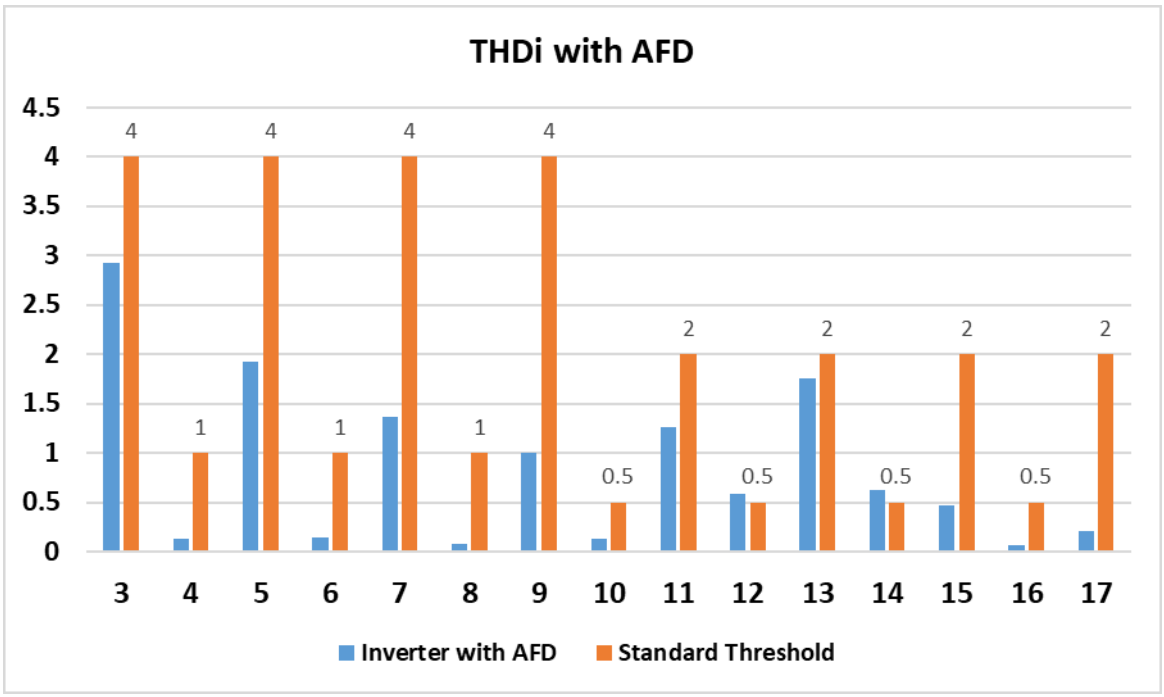
Finally, in order to ensure each individual harmonic recommendation of the Standards were respected, Figures 5.12 to 5.17, compare the harmonic orders obtained after each method implementation with the respective threshold.

Figure 5.11 – Individual harmonic distortion compared with the standards thresholds under no active AIP.



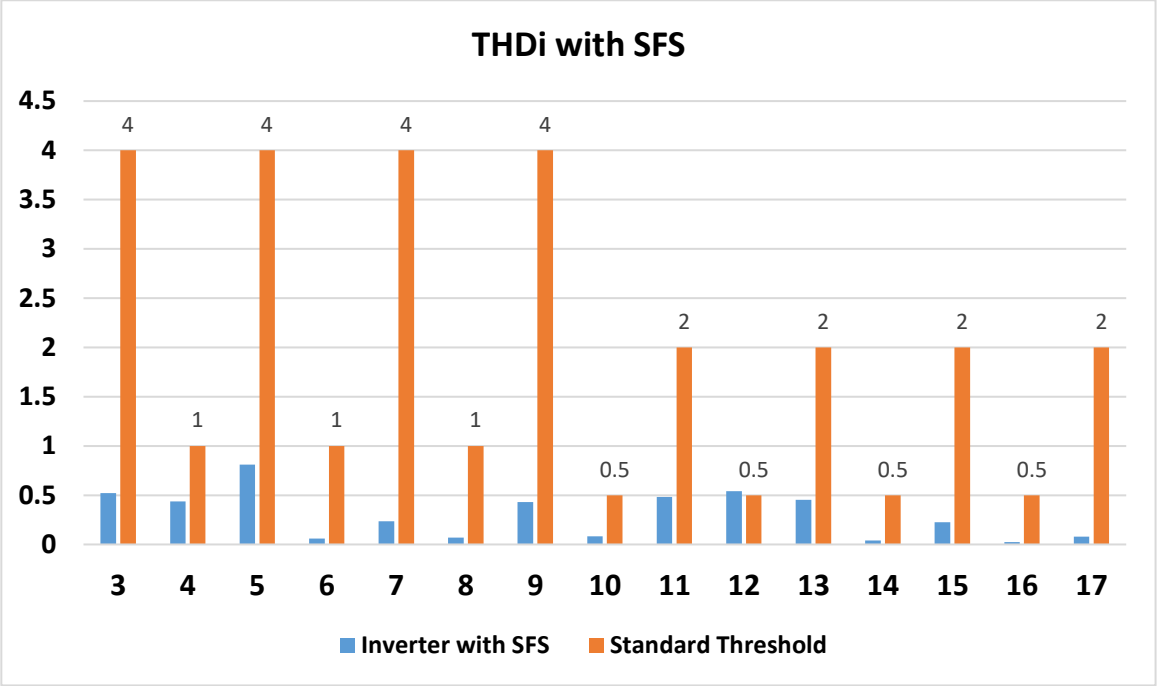
Source: Author.

Figure 5.12 – Individual harmonic distortion under AFD compared with the standards thresholds.



Source: Author.

Figure 5.13 – Individual harmonic distortion under SFS compared with the standards thresholds.



Source: Author.

Figure 5.14 – Individual harmonic distortion under AFDPCF compared with the standards thresholds.

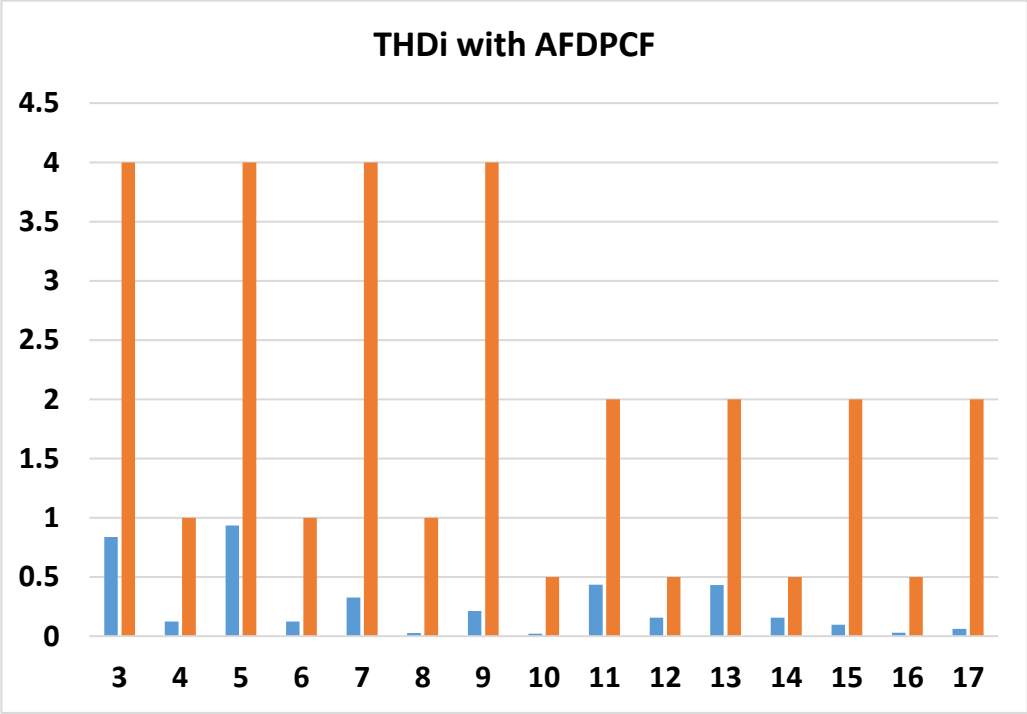
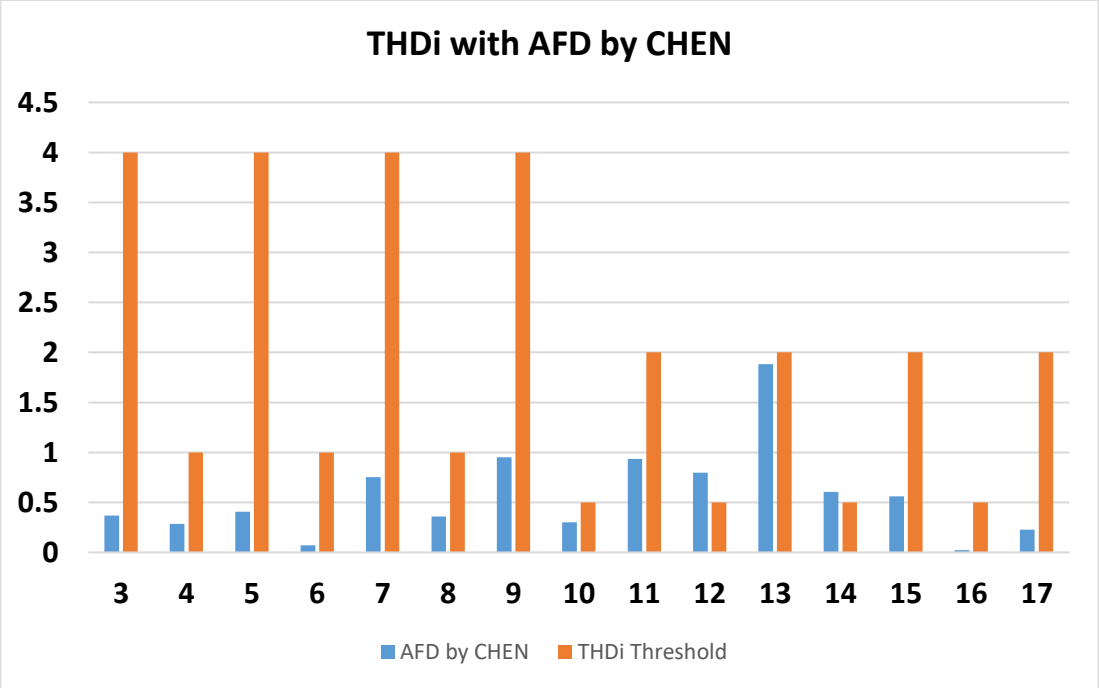
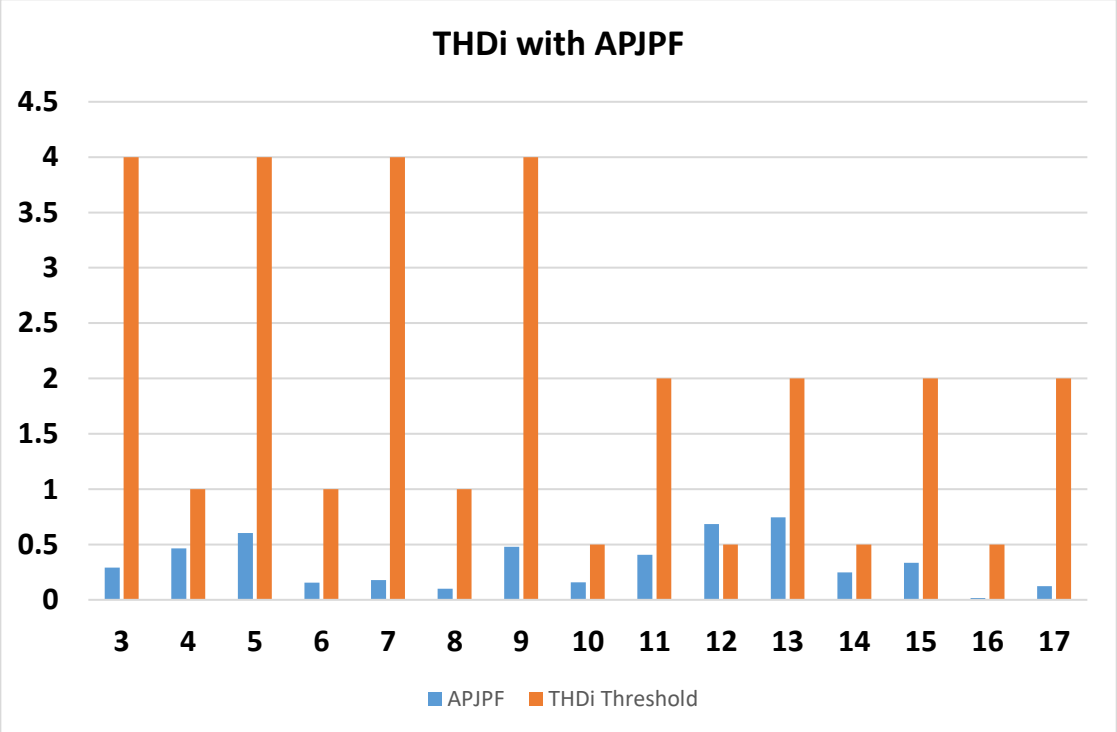


Figure 5.15 – Individual harmonic distortion under AFD by (CHEN et al., 2013) compared with the standards thresholds.



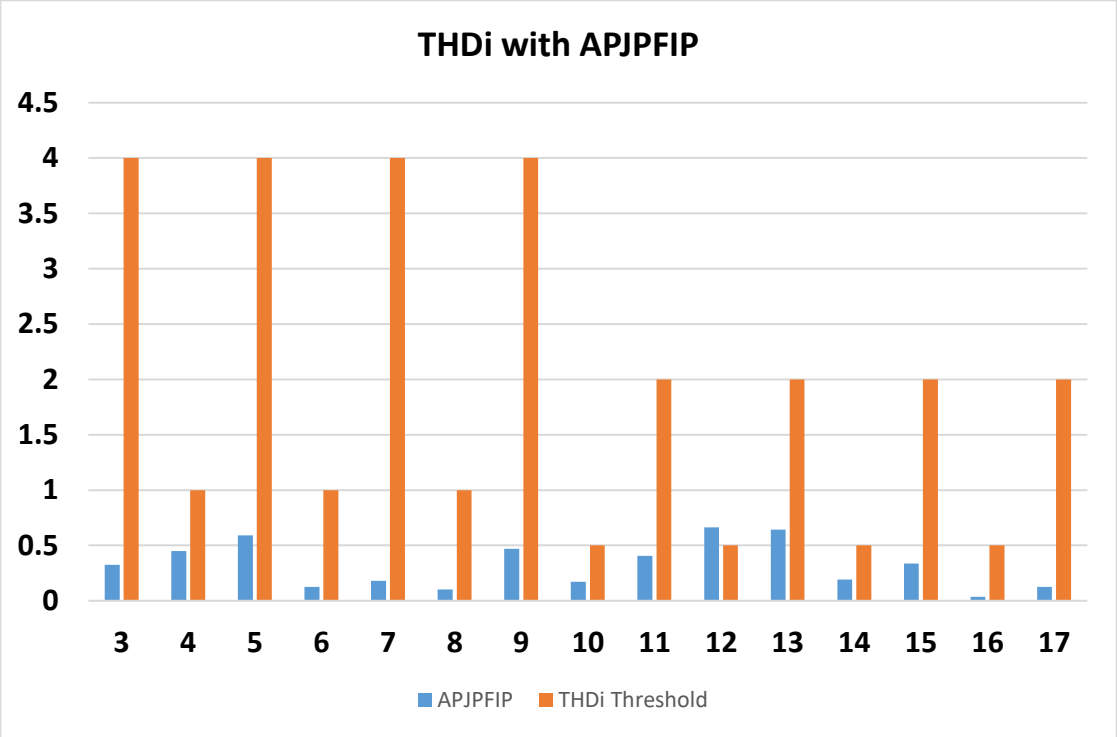
Source: Author.

Figure 5.16 – Individual harmonic distortion under APJPF compared with the standards thresholds.



Source: Author.

Figure 5.17 – Individual harmonic distortion under APJPFIP compared with the standards thresholds.



Source: Author.

5.7 Real Time Results: One Inverter

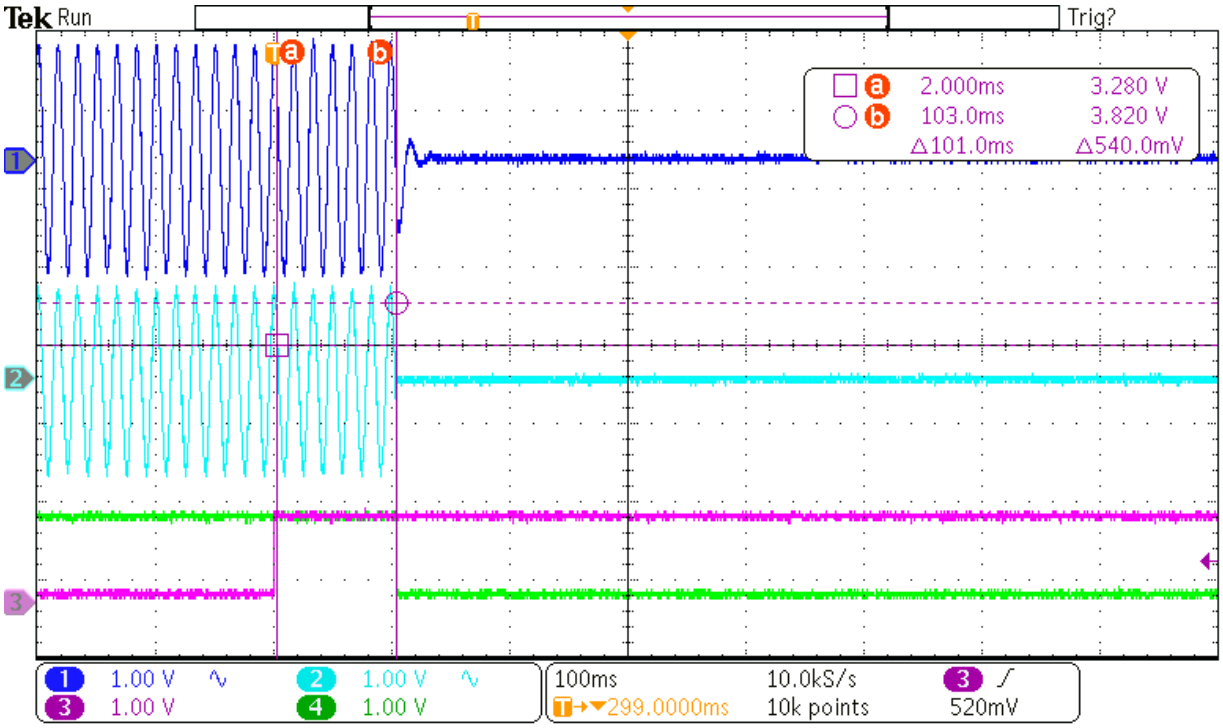
This section will cover the main results of detection time achieved by each of the analyzed strategies. It will provide a comparative analysis between the proposed AIP technique and other well-known strategies in the literature. The results for this case were obtained with one inverter connected to the PCC by a switch. These switches provide physical isolation of the DGS system in case of abnormal operational conditions. They are controlled by the "TRIP" signal and will open after islanding is recognized by the protection system.

The results obtained in a single-inverter context are important in order to compare the performance of the proposed strategy with the other implemented methods. The test battery will cover three values of quality factor ($\boldsymbol{Q_f = 1, Q_f = 2.5}$ and $\boldsymbol{Q_f = 5}$) and different values of normalized capacitance. The variation of quality factor is justified because it affects the selectivity of the RLC circuit and, therefore, the frequency response as stated in (RESENDE; SIMÕES; FREITAS, 2024). Normalized capacitance, in turn, it is critical in relation to NDZ. As illustrated in Section 4.6, the more the value of $\boldsymbol{C_{norm}}$ come closer to unity the nearer the AIP solution will be of its NDZ.

All the tests followed a strict procedure in which the switch that controls the connection of the grid to the PCC is triggered by the "Islanding" signal, which is generated by the DSP, guaranteeing the standardization of the islanding occurrence. This signal is low when the grid is connected and high after grid interruption. The inverter shutdown, in turn, is performed by the "TRIP" signal which is produced by the DSP and present low level for normal operation and high voltage level after islanding is confirmed.

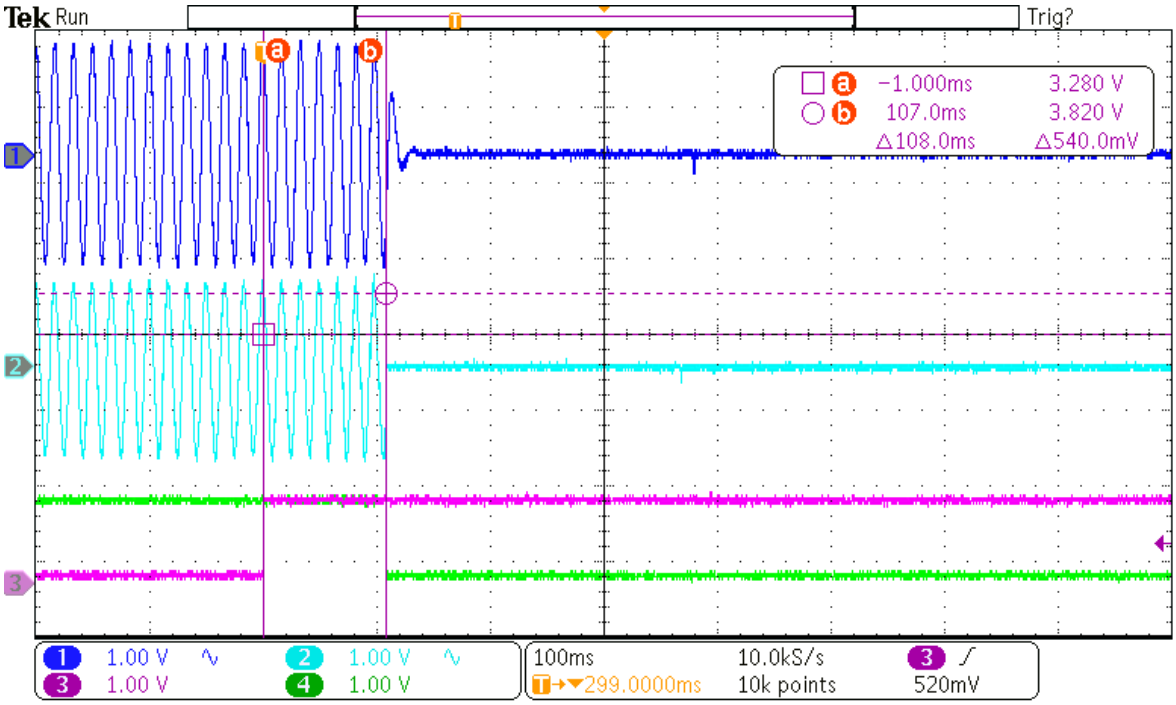
Figures 5.18 to 5.23 illustrate the obtained islanding detection results reached by each method. All of them are composed by voltage, current, islanding and Trip signals for a grid interruption with $\boldsymbol{C_{norm} = 1}$ and $\boldsymbol{Q_f = 1}$. Between the results of this case, the APFJPIP reached the fastest detection time with 71ms. The other results will not be shown in graphical form in order to avoid redundancy.

Figure 5.18 – AFD islanding result for unitary quality factor and normalized capacitance in single inverter.



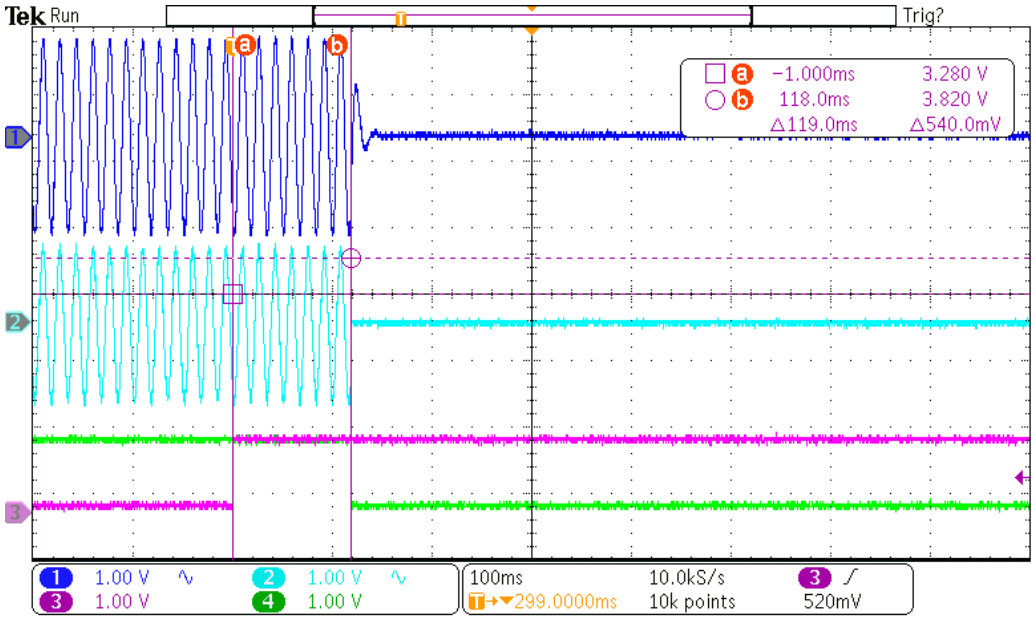
Source: Author.

Figure 5.19 – AFD by Chen islanding result for unitary quality factor and normalized capacitance in single inverter.



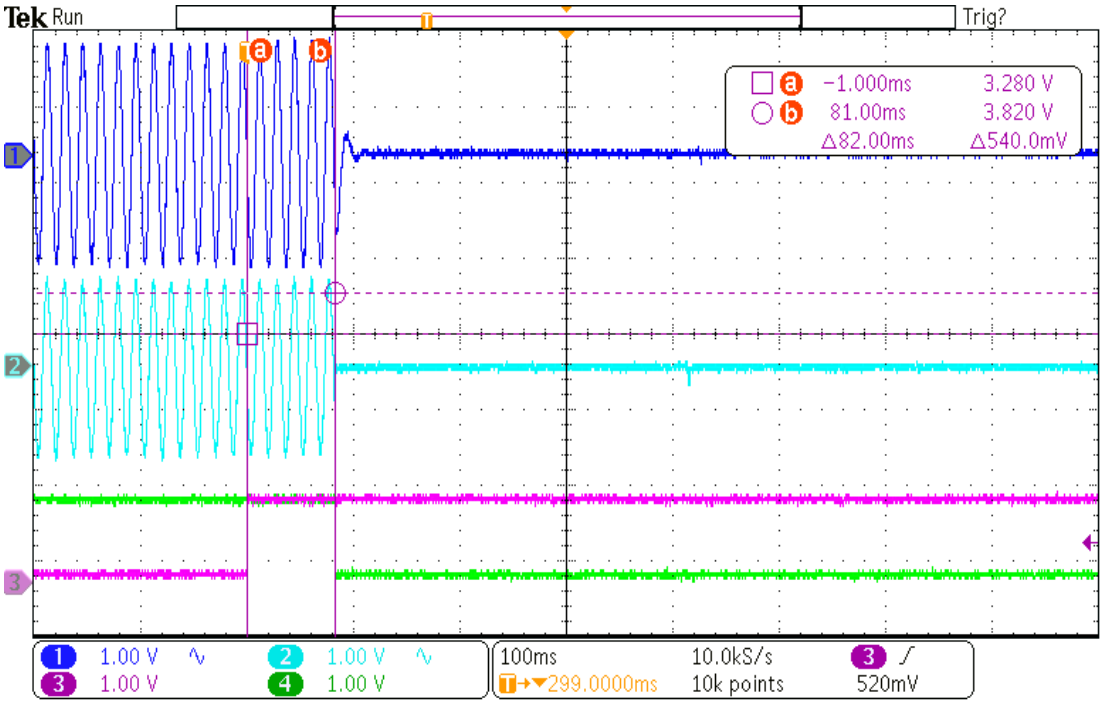
Source: Author.

Figure 5.20 – AFDPCF islanding result for unitary quality factor and normalized capacitance in single inverter.



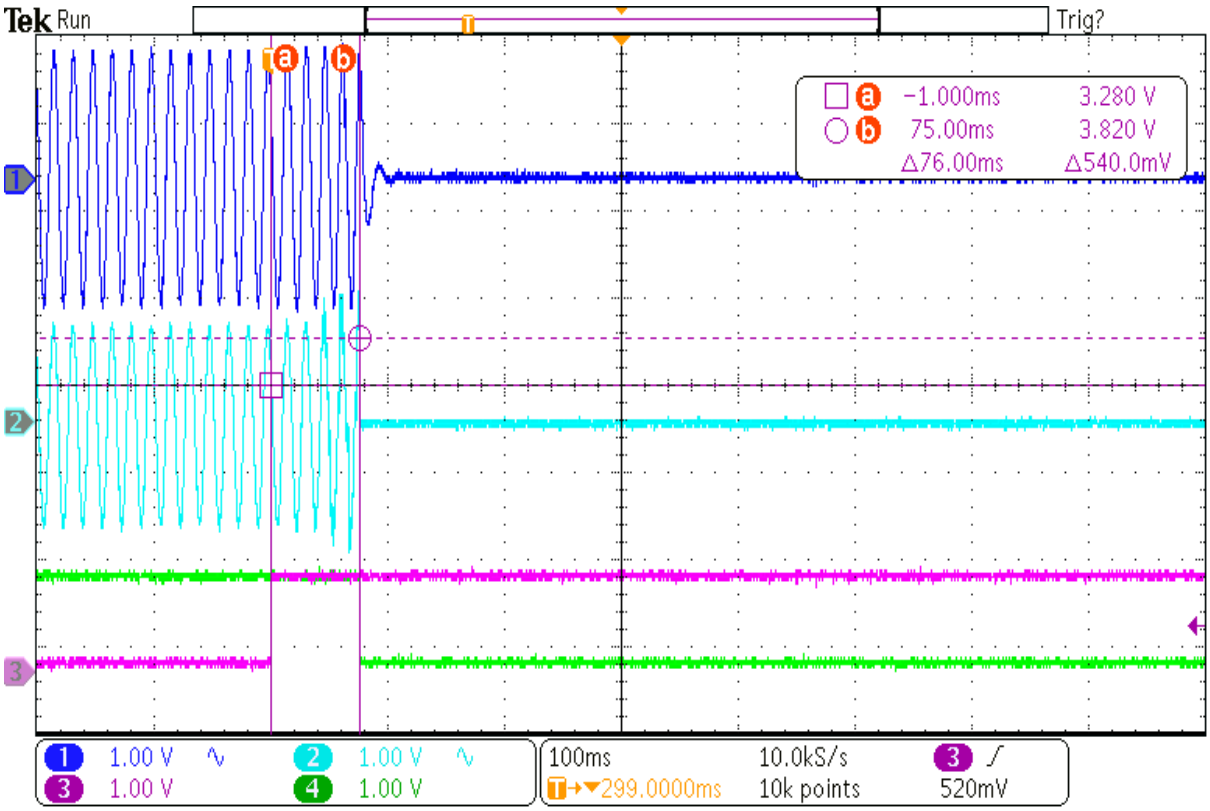
Source: Author.

Figure 5.21 – SFS islanding result for unitary quality factor and normalized capacitance in single inverter.



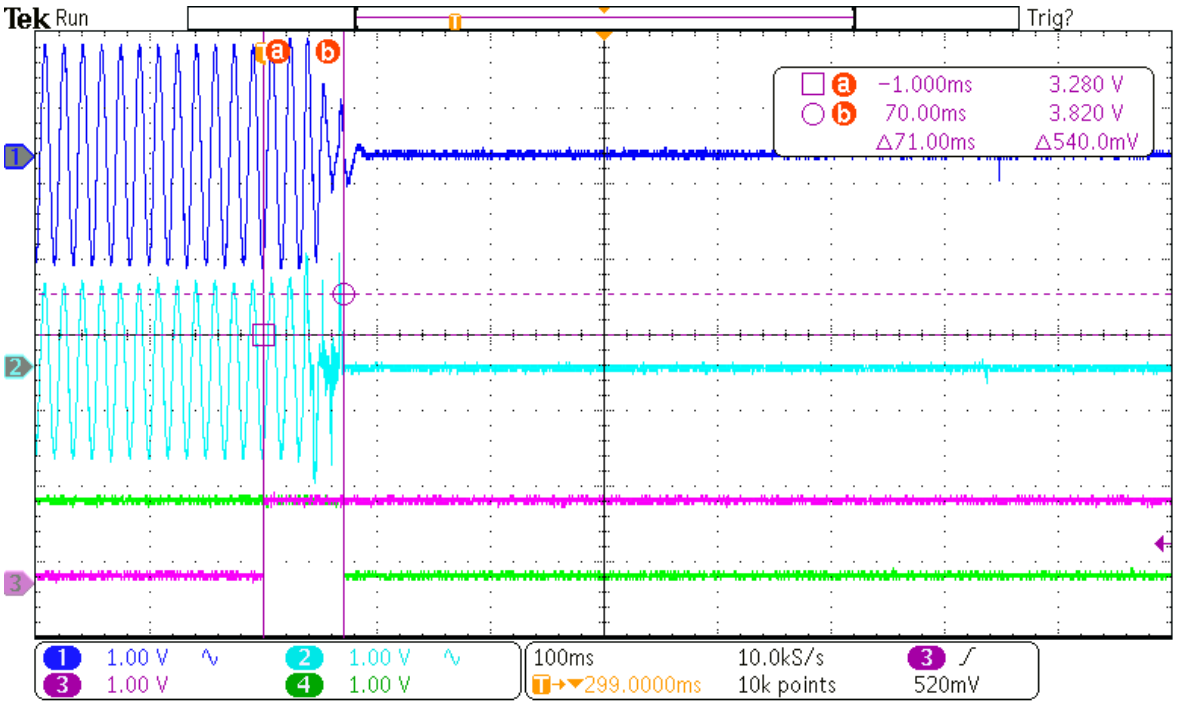
Source: Author.

Figure 5.22 – APJPF islanding result for unitary quality factor and normalized capacitance in single inverter.



Source: Author.

Figure 5.23 – APJPFIP islanding result for unitary quality factor and normalized capacitance in single inverter.



Source: Author.

The following subsection will include graphs that compile detection time results for each selected quality factor. Detection times for each method will be shown across different normalized capacitance values. If a method's result is missing for a specific normalized capacitance value, this signifies that the method has entered a NDZ case. The same considerations can be generalized for sections 5.81, 5.9.1 and 5.10.1.

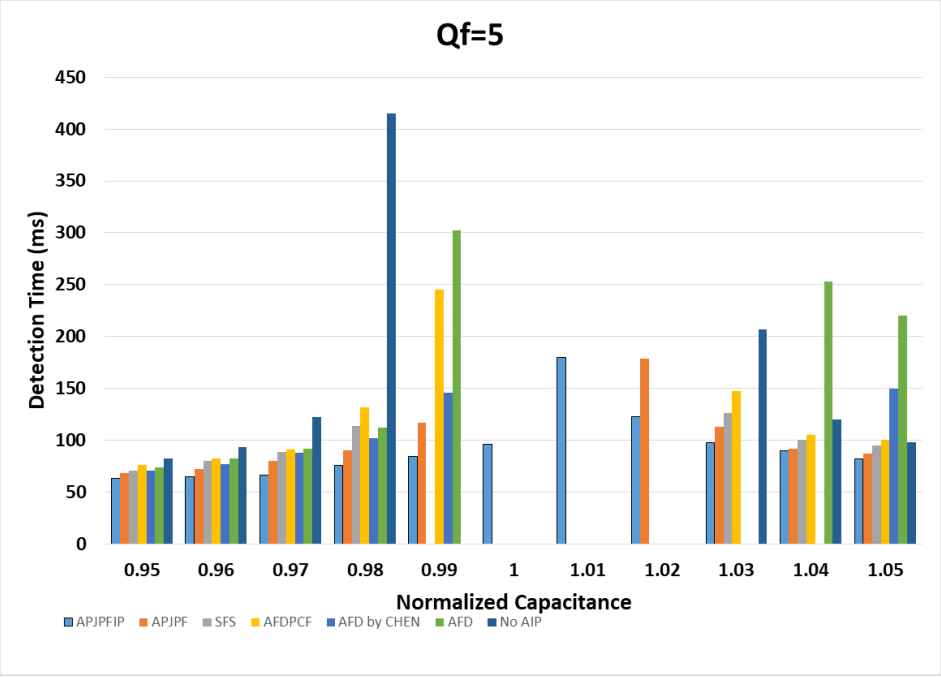
5.7.1 Time Detection Comparison.

It is crucial to compare the results within the same graph to verify the claimed reduction in detection time achieved by the proposed solution. Accordingly, Figure 5.24 shows the detection times for each of the compared strategies at $Q_f = 1$. Generally, all methods provided quick and accurate islanding detection for more inductive loads. However, for more capacitive loads, there is a clear trend of increased detection time in the AFD and AFD methods (CHEN et al., 2013). It's important to note that these methods have fixed parameters, which allow them to follow the frequency drift tendency imposed by the local load characteristics. For instance, in the case of AFD, detection time consistently increases from 71 ms at $C_{norm} = 0.95$ to 165ms at $C_{norm} = 1.02$. For the subsequent capacitance conditions, the method falls in the NDZ.

The best results were obtained by the APJPFIP for all the tested cases. It also reached the lowest detection time among the analyzed methods, i.e, 60 ms for $C_{norm} = 0.95$ and the lowest average detection time.

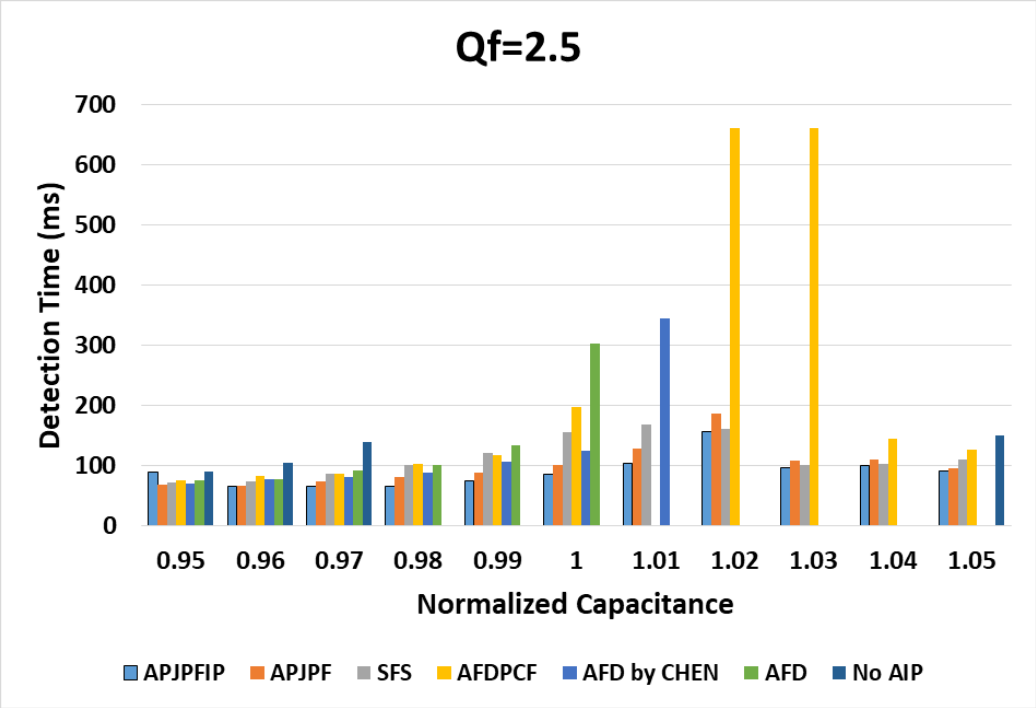
Figure 5.25 and 5.26 illustrates the detection times reached by each strategy for $Q_f = 2.5$ and $Q_f = 5$, respectively. Generally, all methods performed rapid and accurate islanding detection for more inductive loads. For all of the tested cases, for both quality factors values, the proposed method reached faster detection. Moreover, it was the only method that did not incurred in NDZ for all the tested cases. For $Q_f = 2.5$, however, the AFDPCF incurred in one NDZ case, the AFD by (CHEN et al., 2013) in 4 and the Classic AFD in 5. For $Q_f = 5$, APJPF presented 2 NDZ cases, SFS presented 4, AFDPCF presented 3, AFD by (CHEN et al., 2013) 5 and the Classic AFD 4. Beyond that, the proposed method presented the smallest average detection time. It is important to highlight that the values of the series called "No AIP" were obtained with the inverter operating with no active islading protection scheme.

Figure 5.24 – Comparison of the detection time for $Q_f = 1$.



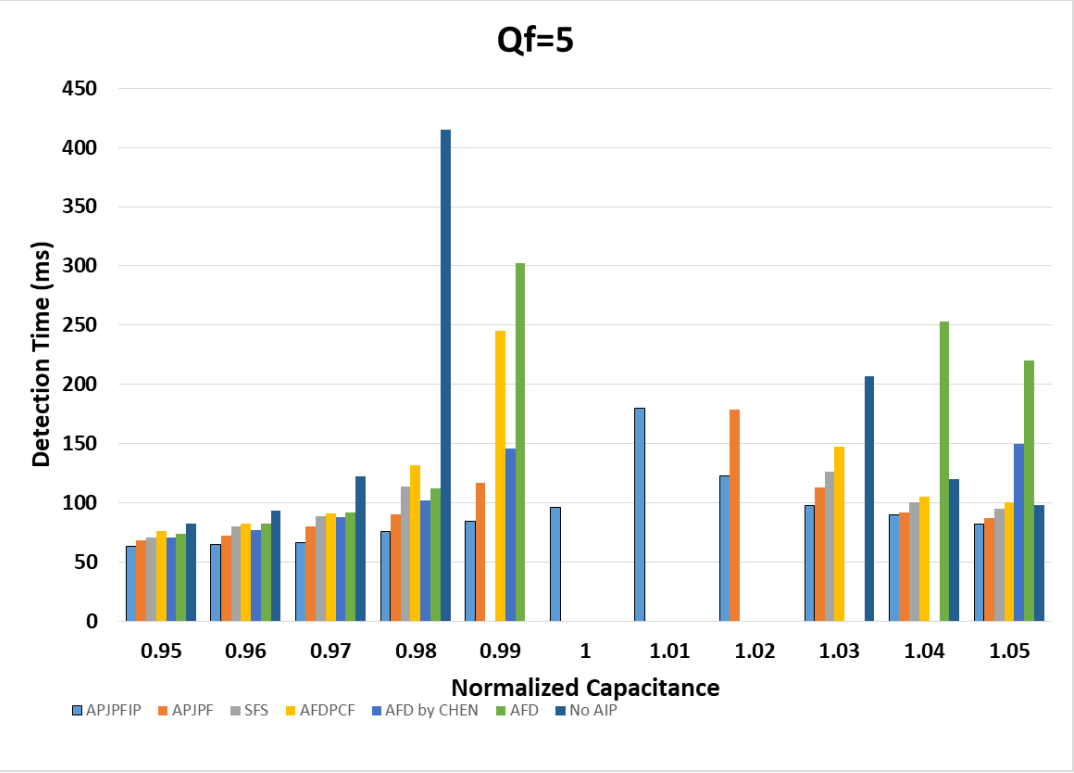
Source: Author.

Figure 5.25 – Comparison of the detection time for $Q_f = 2.5$.



Source: Author.

Figure 5.26 –



Comparison of the detection time for $Q_f = 2.5$.

Source: Author.

Finally, all the obtained results and all the information provided over the text of this section are summarized in Table 5.1.

Table 5.1 – Detection time results for single inverter environment.

Qf=1	***Cnorm***	***Methods***						
		APJPFIP	**APJPF**	**SFS**	**AFDPCF**	**AFD by Chen**	**AFD**	**No AIP**
	0.95	60	66	67	73	68	71	111
	0.96	62	65	70	73	66	75	142
	0.97	61	65	73	86	75	78	505
	0.98	62	70	82	540	75	87	NDZ
	0.99	67	67	91	98	79	91	NDZ
	1	71	76	82	117	108	101	NDZ
	1.01	70	73	100	124	89	121	NDZ
	1.02	80	90	115	137	99	165	NDZ
	1.03	86	115	109	316	104	NDZ	NDZ
	1.04	101	142	150	357	185	NDZ	NDZ
	1.05	96	124	167	384	220	NDZ	176
	Average	67	72	91	137	85	89	159
	NDZ Cases	0	0	0	0	0	3	7
	Cnorm	**APJPFIP**	**APJPF**	**SFS**	**AFDPCF**	**AFD by Chen**	**AFD**	**No AIP**
	0.95	63	68	72	75	70	75	90
	0.96	65	67	74	82	77	78	105
	0.97	65	73	86	86	80	91	139
	0.98	65	80	100	103	88	100	NDZ
	0.99	75	88	120	118	107	133	NDZ
	1	85	100	156	198	125	303	NDZ
	1.01	104	128	168	NDZ	345	NDZ	NDZ
	1.02	157	186	160	660	NDZ	NDZ	NDZ
	1.03	96	108	100	660	NDZ	NDZ	NDZ
	1.04	100	110	103	144	NDZ	NDZ	NDZ
	1.05	90	95	110	126	NDZ	NDZ	150
	Average	89	95	103	122	88	95.5	122
	NDZ Cases	0	0	0	1	4	5	7
Qf=5	**Cnorm**	**Methods**						
		APJPFIP	**APJPF**	**SFS**	**AFDPCF**	**AFD by Chen**	**AFD**	**No AIP**
	0.95	63	68	71	76	71	74	82
	0.96	65	72	80	82	77	82	93
	0.97	66	80	89	91	88	92	122
	0.98	76	90	114	132	102	112	415
	0.99	84	117	NDZ	245	146	302	NDZ

	1	96	NDZ	NDZ	NDZ	NDZ	NDZ	NDZ
	1.01	180	NDZ	NDZ	NDZ	NDZ	NDZ	NDZ
	1.02	123	179	NDZ	NDZ	NDZ	NDZ	NDZ
	1.03	98	113	126	147	NDZ	NDZ	207
	1.04	90	92	100	105	NDZ	253	120
	1.05	82	87	95	100	150	220	98
	Average	84	90	95	102.5	95	112	120
	NDZ Cases	0	2	4	3	5	4	4

Source: Author.

5.8 Real Time Results: Double-Inverter

This sixth section of this document will discuss the results for a double inverter DGS. The importance of this kind of test is well described in technical research. As the active methods insert some disturbances into the PCC, it is important to evaluate how different active methods interact with others. The theoretical analysis done in Chapter 3 showed that the detection capabilities some strategies based in frequency drift and harmonic distortion are highly impacted by the number of inverters connected to the islanded system.

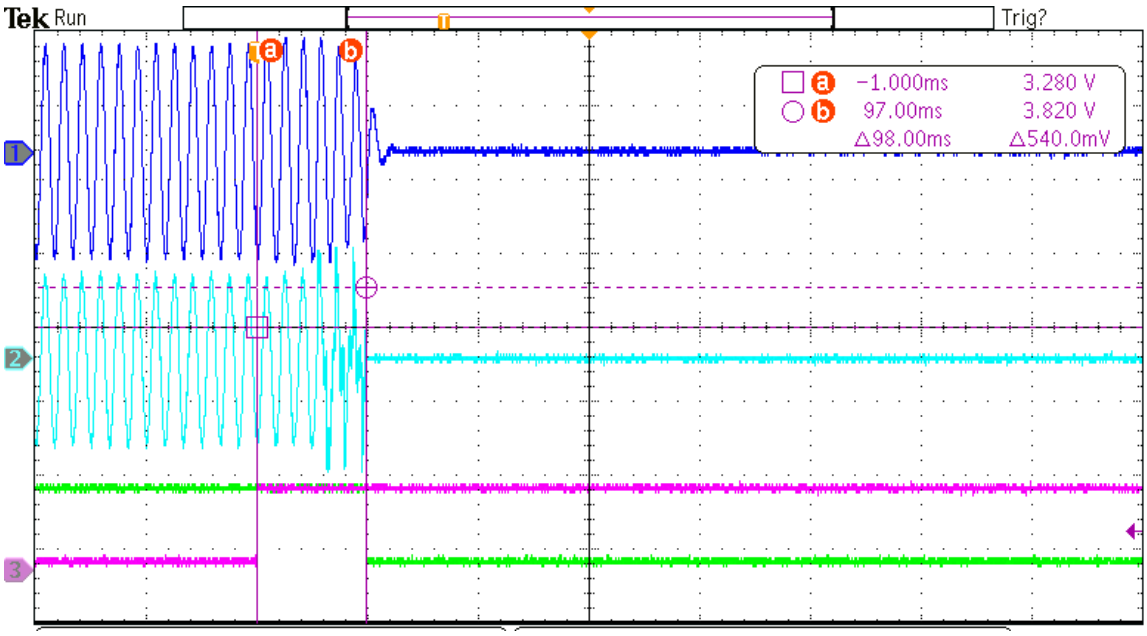
Thus, this section will evaluate the performance of the proposed strategy working in parallel with other active solutions. There will be seven combinations in which one of the inverter units will be equipped with the APJPFIP and the other will work or without active AIP or with one of the other known strategies. The obtained results will be compared with the islanding detection times reached by the methods in the single-inverter case, proving that the proposed solution is not only suitable for working with different strategies but also improves the performance of the methods.

The test battery will cover three values of quality factor ($\boldsymbol{Q_f = 1}$, $\boldsymbol{Q_f = 2.5}$ and $\boldsymbol{Q_f = 5}$) and different values of normalized capacitance. The same considerations related to the importance of quality factor and normalized capacitance variation done for single inverter environment can be also generalized for this case. The signals “Islanding” and “TRIP” are generated by the DSP and indicate the moment of grid interruption and the inverter shutdown, respectively.

Figures 5.27 to 5.33 illustrate the obtained islanding detection results reached by each method. All of them are composed by voltage, current, islanding and Trip signals for a grid

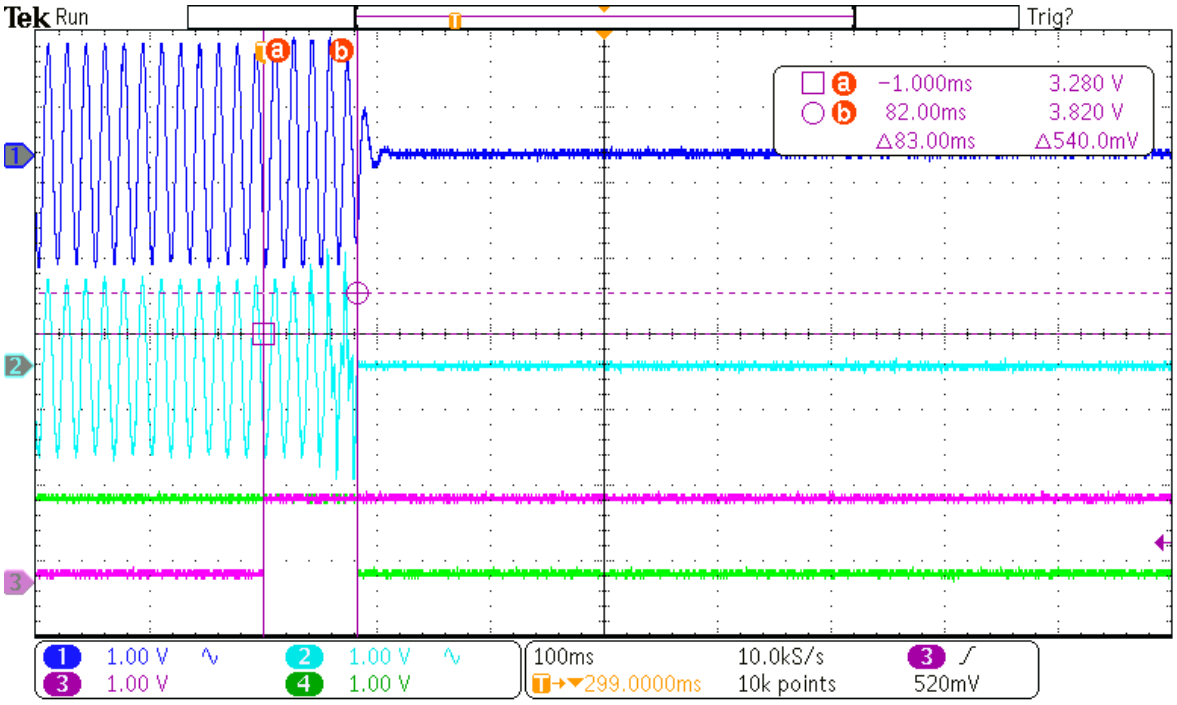
interruption with $C_{norm} = 1$ and $Q_f = 1$. Between the results of this case, the APFJPIP reached fastest detection with 72ms.

Figure 5.27 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2: No AIP.



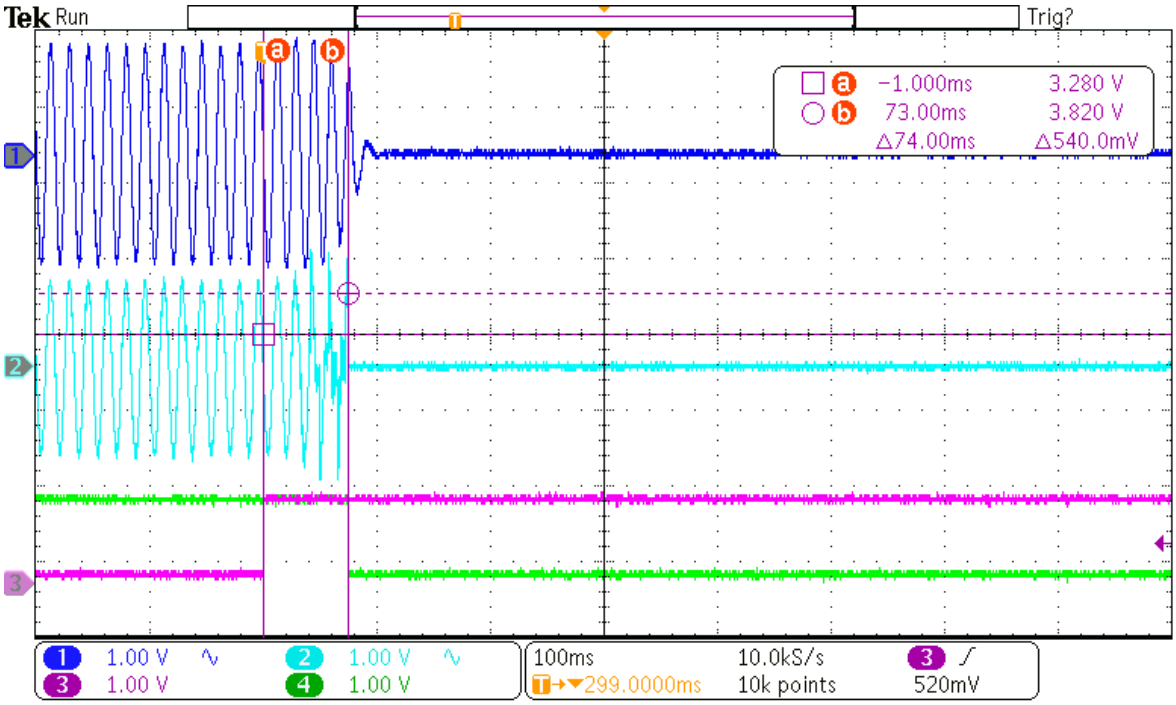
Source: Author.

Figure 5.28 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2: No AFD.



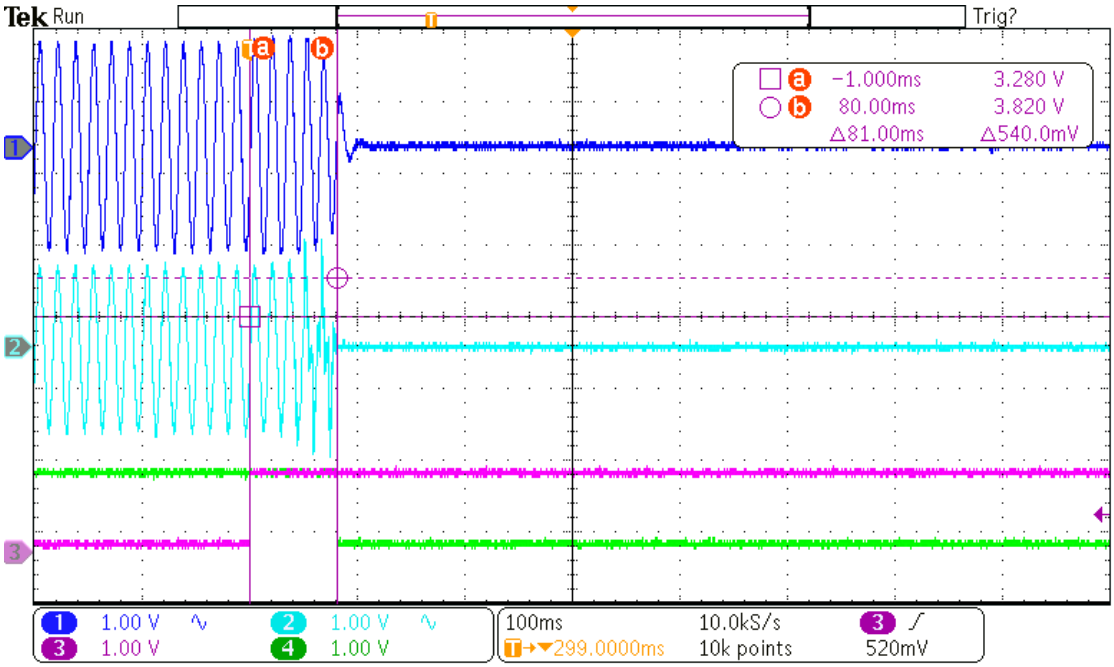
Source: Author.

Figure 5.29 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2: AFD by (CHEN et al, 2013).



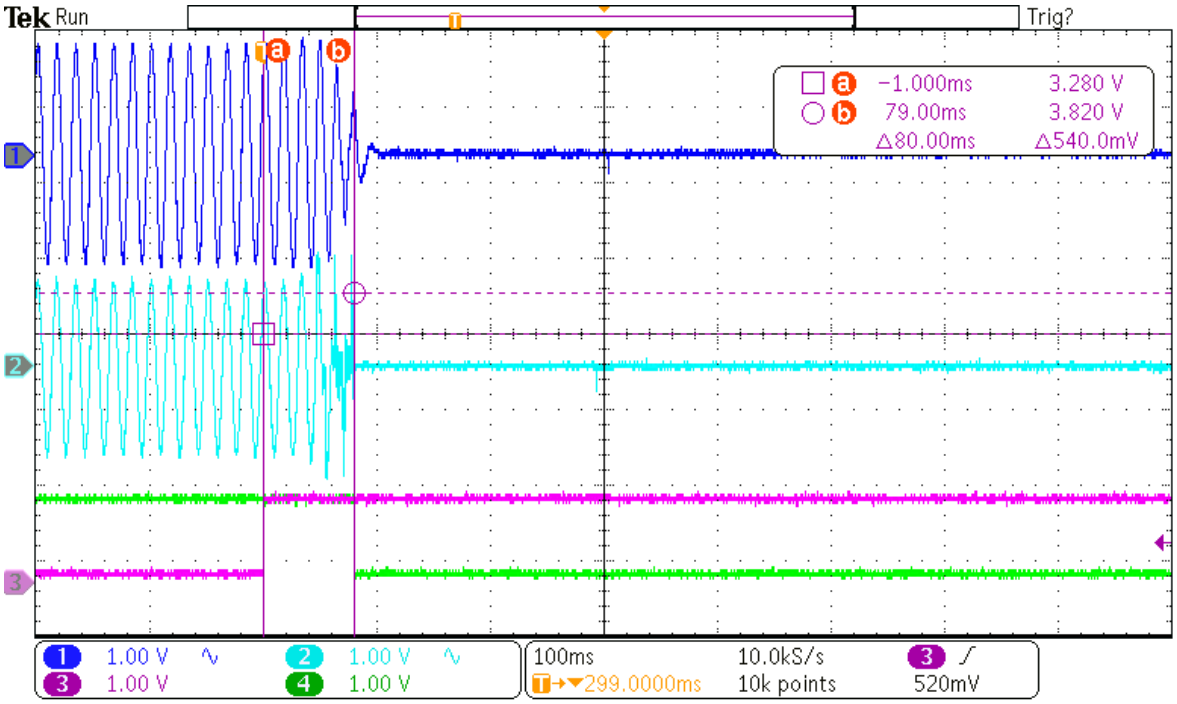
Source: Author.

Figure 5.30 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2: AFDPCF.



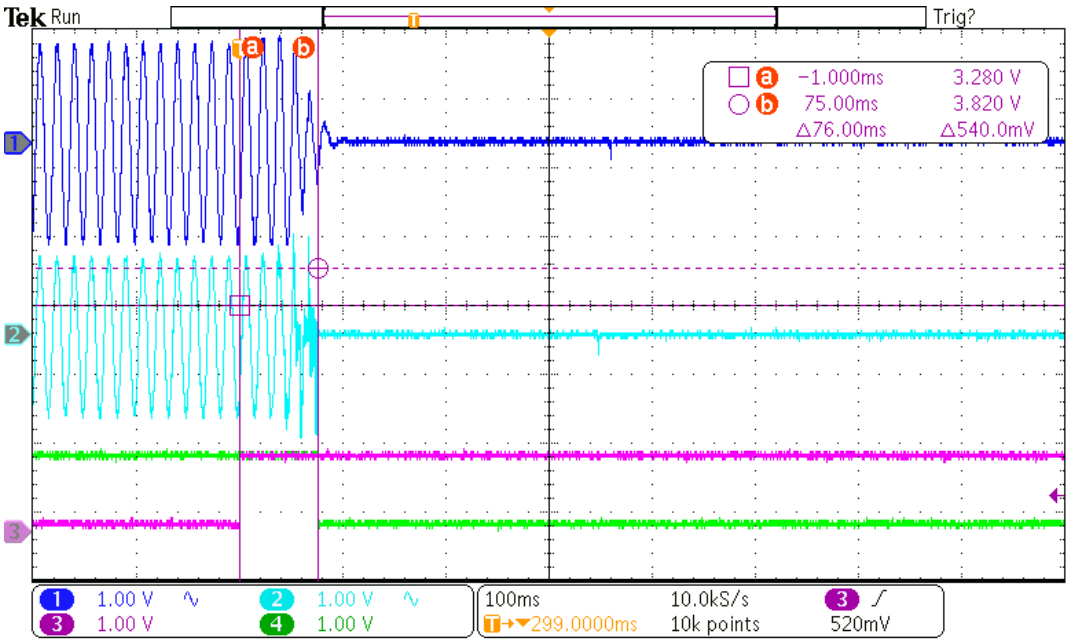
Source: Author.

Figure 5.31 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2: SFS.



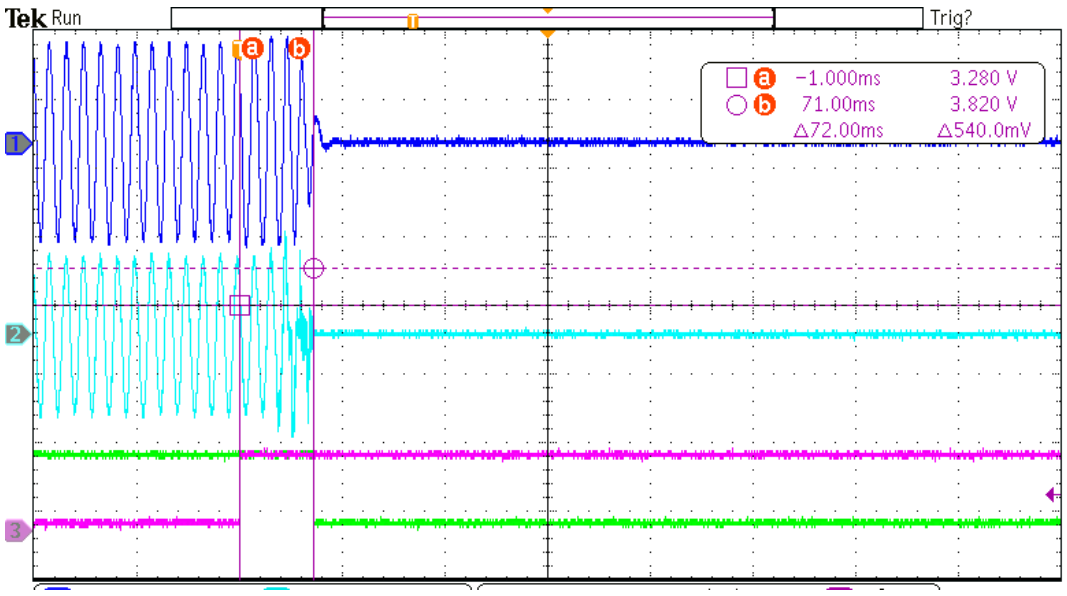
Source: Author.

Figure 5.32 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2: APJPF.



Source: Author.

Figure 5.33 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2: APJPFIP.



Source: Author.

5.8.1 Time Detection Comparison.

The presented results confirm the effectiveness of the proposed solution working in parallel with the other known AIP methods. However, it is necessary to compare the detection time reached when both inverters are equipped with the APJPFIP with the other results reached by those methods when working in a single DG environment. In this sense, Figures 5.34, 5.35 and 5.36 demonstrate the results of detection time for $Q_f = 1$, $Q_f = 2.5$ and $Q_f = 5$.

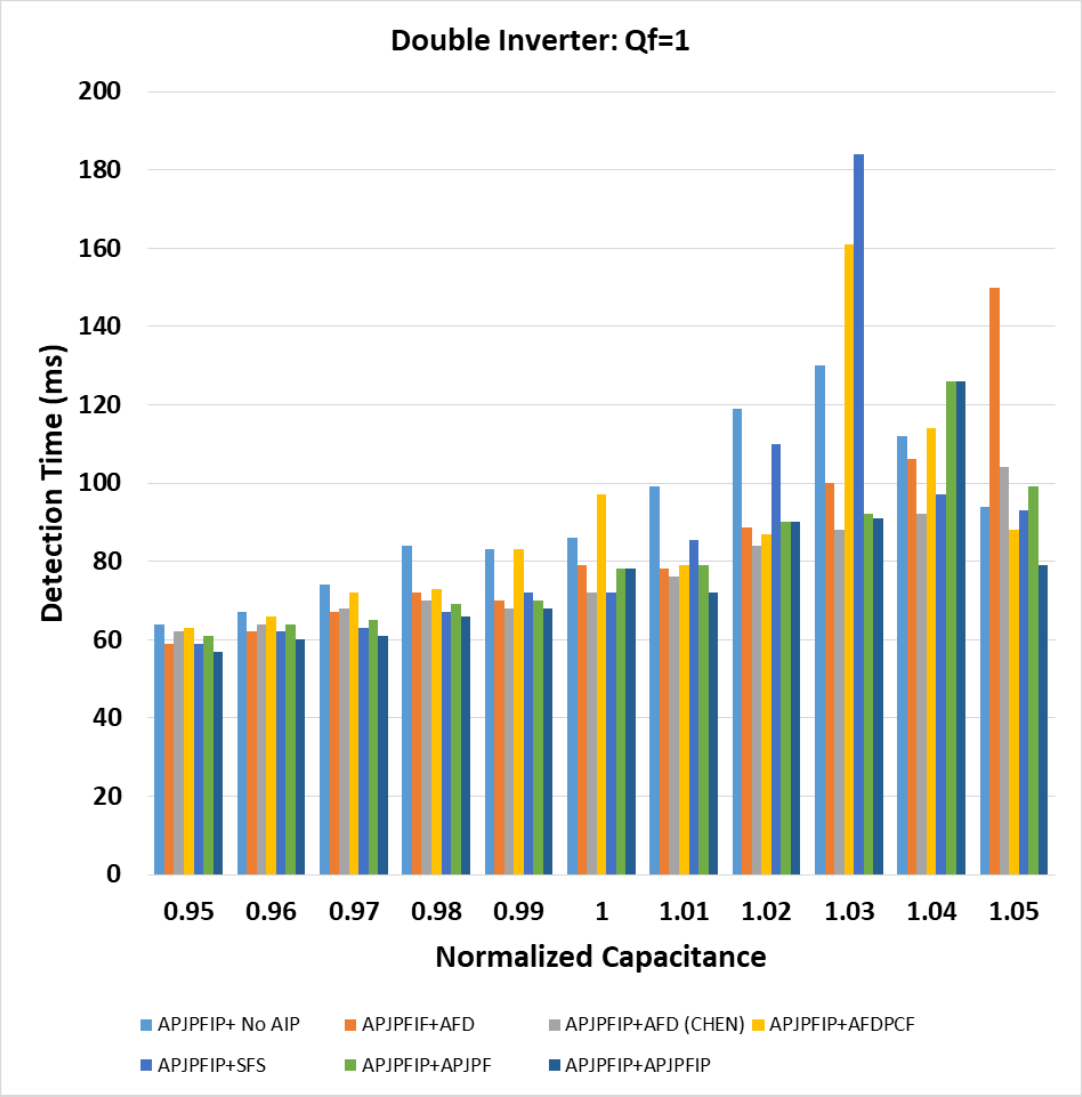
The main obtained results indicate the following:

- The passive AIP presented 18 NDZ cases in single inverter and no NDZ case working in parallel with the proposed solution. The average detection time was 159ms ($Q_f = 1$), 122ms ($Q_f = 2.5$) and 120ms ($Q_f = 5$). The detection time obtained for each value of normalized capacitance was lower than for the inverter working with no active AIP in single-inverter mode.
- AFD presented 12 NDZ cases in single inverter, 3 cases for $Q_f = 1$, 4 cases for $Q_f = 2.5$ and 5 for $Q_f = 5$. Working in parallel with the APJPFIP this number was reduced to 1 case for $Q_f = 5$. The average detection time was 159ms ($Q_f = 1$), 122ms ($Q_f = 2.5$) and 120ms ($Q_f = 5$). The average detection times were, respectively, 84ms, 96.6ms and 97ms. The detection time was lower for all the tested cases if compared with AFD in single DG configuration.

- AFD by (CHEN et al., 2013) resulted in 3 NDZ cases for $Q_f = 1$, 5 cases for $Q_f = 2.5$, and 4 cases for the condition in which $Q_f = 5$. Additionally, the average detection times were 85ms, 88ms, and 95ms, respectively. However, when operating in parallel with an inverter equipped with the APJPFIP, no NDZ cases were observed. The average detection times were 78ms, 92ms, and 139ms, respectively. The detection time was lower for all the tested cases if compared with the AFD by (CHEN et al., 2013) in single DG configuration.
- With only one inverter, AFDPCF led to 1 NDZ case for $Q_f = 2.5$ and 3 cases for the condition in which $Q_f = 5$. It presented 137ms, 122ms and 102.5ms of average time detection. Working in parallel with an inverter equipped with the APJPFIP, on the other hand, it presented no NDZ case. The average detection times were, respectively, 89ms, 98ms and 110ms. The detection time was lower for all the tested cases if compared with the AFDPCF working in single-DG configuration.
- In single-inverter mode, SFS leads to 4 NDZ cases for $Q_f = 5$. It presented 91ms, 103ms and 95ms of average time detection. Working in parallel with an inverter equipped with the APJPFIP, on the other hand, it presented no NDZ case. The average detection times were, respectively, 88ms, 90ms and 102ms. The detection time was lower for all the tested cases if compared with the SFS working in single-DG configuration.
- In the scenario with only one inverter, APJPF leads to 2 NDZ cases for $Q_f = 5$. It presented 72ms, 95ms and 90ms of average time detection. Working in parallel with an inverter equipped with the APJPFIP, on the other hand, it presented no NDZ case. The average detection times were, respectively, 81ms, 91ms and 95ms. The detection time was lower for all the tested cases if compared with the APJPF working in single-DG configuration.

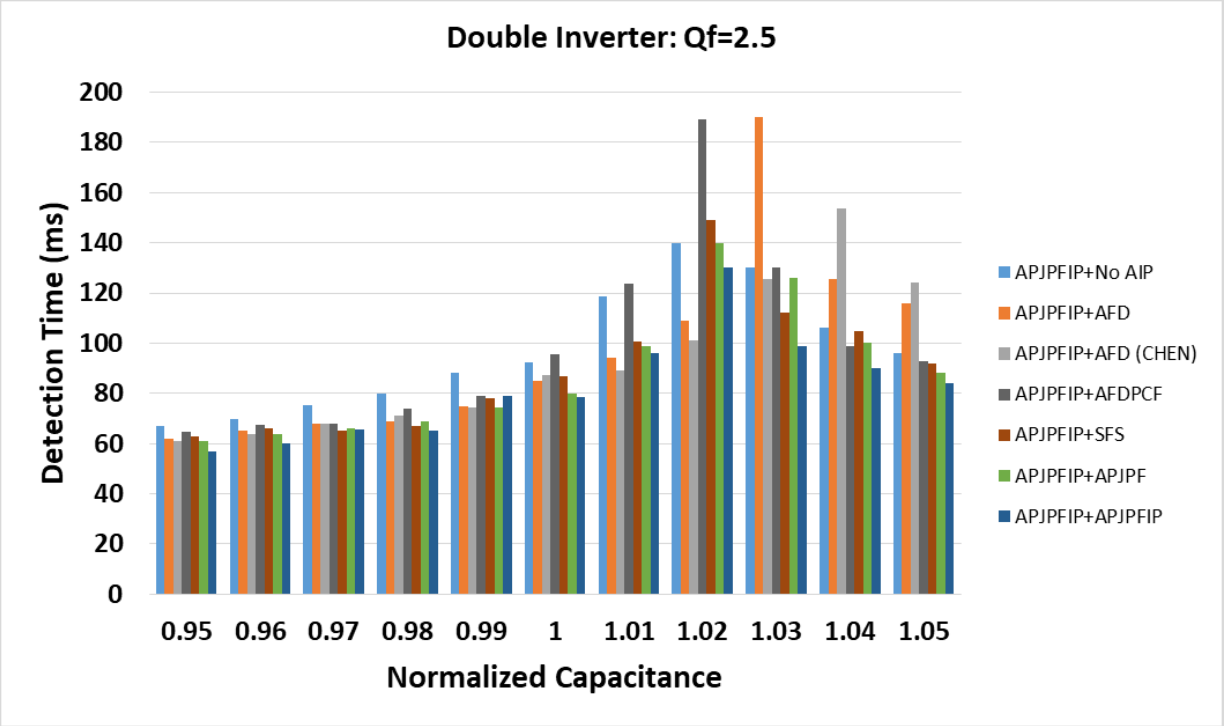
Finally, table 5.2 condenses all the obtained results for the double inverter scenario.

Figure 5.34 – Comparison of the detection time for $Q_f = 1$ for double inverter scenario.



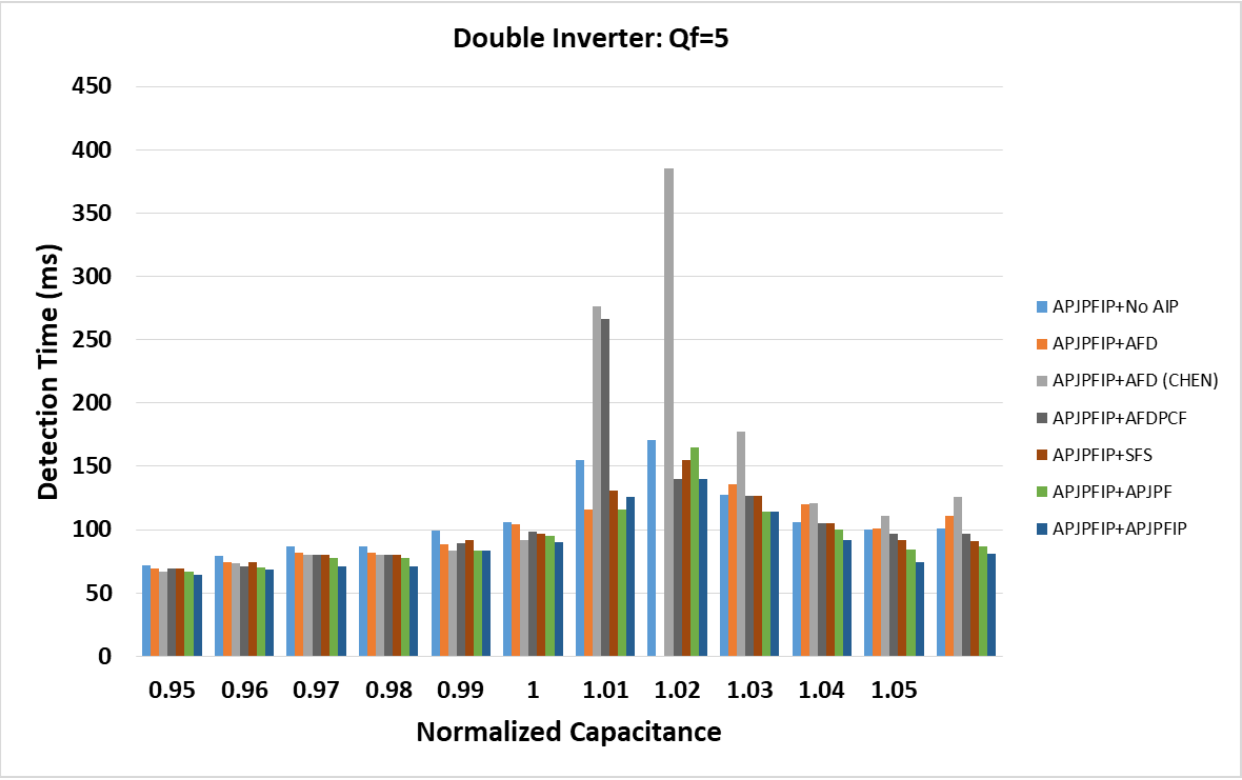
Source: Author.

Figure 5.35 – Comparison of the detection time for $Q_f = 2.5$ for double inverter scenario.



Source: Author.

Figure 5.36 – Comparison of the detection time for $Q_f = 5$ for double inverter scenario.



Source: Author.

Table 5.2 – Detection time results for double inverter environment.

Qf=1	*Cnorm*	*Methods*						
		APJPFIP	**APJPF**	**SFS**	**AFDPCF**	**AFD by Chen**	**AFD**	**No AIP**
	0.95	58	61	59	63	61	60	64
	0.96	62	64	62	66	64	62	67
	0.97	62	65	63	72	67	68	74
	0.98	64	69	67	73	69	70	84
	0.99	72	70	72	83	70	72	82
	1	72	76	80	81	74	83	98
	1.01	78	79	85.5	79	70.5	78	99
	1.02	88	90	110	87	75	88.5	119
	1.03	80	92	184	161	80	100	130
	1.04	88	126	97	114	106	106	112
	1.05	82	99	93	88	130	150	94
	Average	73	81	88	89	79	85	93
	NDZ Cases	0	0	0	0	0	0	0
	Cnorm	**APJPFIP**	**APJPF**	**SFS**	**AFDPCF**	**AFD by Chen**	**AFD**	**No AIP**
	0.95	60	61	63	64.5	61	62	67
	0.96	62	64	66	67.5	64	65	70
	0.97	64	66	65	68	68	68	76
	0.98	72	69	67	74	71	70	80
	0.99	78	74.5	78	79	74.5	75	88
	1	98	80	87	95.5	87.5	85	92.5
	1.01	122	99	100.5	123.5	89	94	118
	1.02	106	140	149	189	101	109	140
	1.03	86	126	112	130	125.5	190	130
	1.04	80	100	105	99	1535	125.5	106
	1.05	74	88	92	93	124	116	100
	Average	78	80	87	93	87.5	85	92.5
	NDZ Cases	0	0	0	0	0	0	0
Qf=5	**Cnorm**	**Methods**						
		APJPFIP	**APJPF**	**SFS**	**AFDPCF**	**AFD by Chen**	**AFD**	**No AIP**
	0.95	61	66	69	69	66.5	70	72
	0.96	64	70	74	71	73.5	74	79
	0.97	70	78	80	80	80	82	87
	0.98	72	78	80	80	80	88	87
	0.99	86	83	91.5	89	83	104	99.5
	1	102	95	97	98	92	116	106
	1.01	144	116	130	266	276	NDZ	170.5
	1.02	112	165	156	140	385	135.5	127.5
	1.03	92	114	127	127	177	120	106
	1.04	92	100	105	105	121	101	100
	1.05	76	84	92	97	111	112	101

	Average	86	87	90.5	97	92	102.5	100
	NDZ Cases	0	0	0	0	0	1	0

Table 5.2 – Detection time results for double inverter environment.

Source: Author.

5.9 Triple Inverter Islanding Results

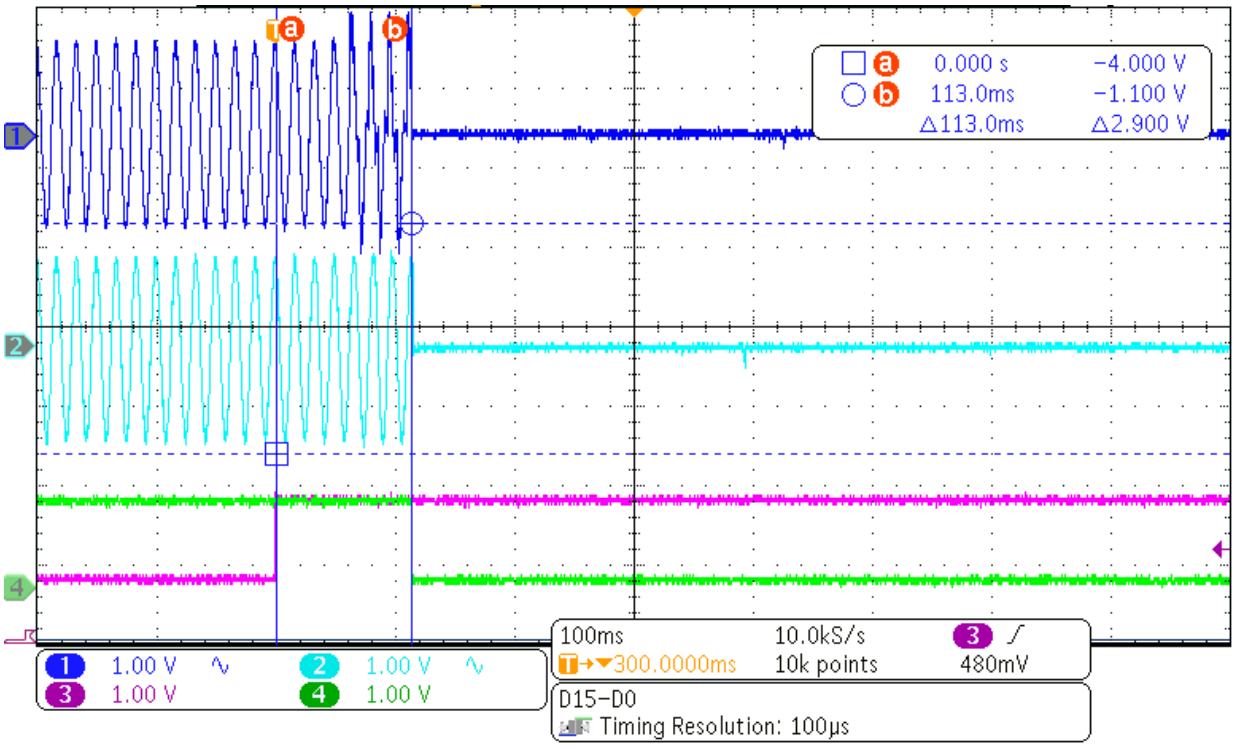
This section presents the results for a triple inverter-based DGS. The goal of these results is to demonstrate that the proposed solution aligns with modern research on microgrids. Although this document does not cover the topic of microgrids, the islanding detection function is an important feature in microgrid systems. It can be applied to detect unintentional islanding and initiate the physical disconnection of the microgrid from the utility grid, as recommended by standards. It also provides information for control transitions from grid-following to grid-forming modes or even for optimizing inverter operation after islanding.

This section will evaluate the performance of the proposed strategy when operating in parallel with other active solutions in a triple inverter-based system. The combinations used will be the same as in the previous section. However, in this case, one inverter will be equipped with the proposed APJPFIP, while the other two will either have no active AIP or will use one of the analyzed solutions. Since the inverters share the same load, the proposed method will demonstrate its detection capabilities even when sharing only 33% of the total generated power. The load will be designed in accordance with standard recommendations.

The test battery will include three different quality factor values ($\boldsymbol{Q_f = 1, Q_f = 2.5}$, $\boldsymbol{Q_f = 5}$), along with varying normalized capacitance values. The observations regarding the significance of quality factor and changes in normalized capacitance made for the single inverter scenario can also be extended to this case. The DSP generates the "Islanding" and "TRIP" signals, which indicate the moments of grid disconnection and inverter shutdown, respectively.

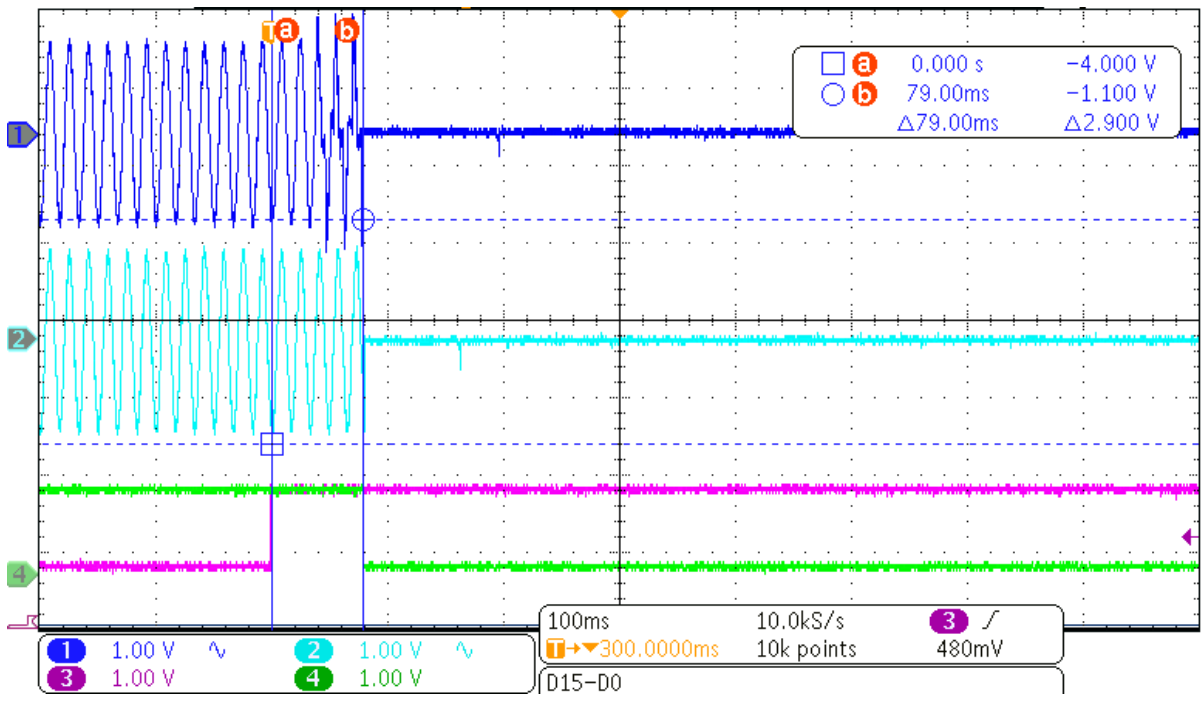
Figures 5.37 to 5.43 illustrate the obtained islanding detection results reached by each method. All of them are composed by voltage, current, islanding and Trip signals for a grid interruption with $\boldsymbol{C_{norm} = 1}$ and $\boldsymbol{Q_f = 1}$. Between the results of this case, the APFJPIP reached fastest detection with 72ms.

Figure 5.37 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2 and 3: No AIP.



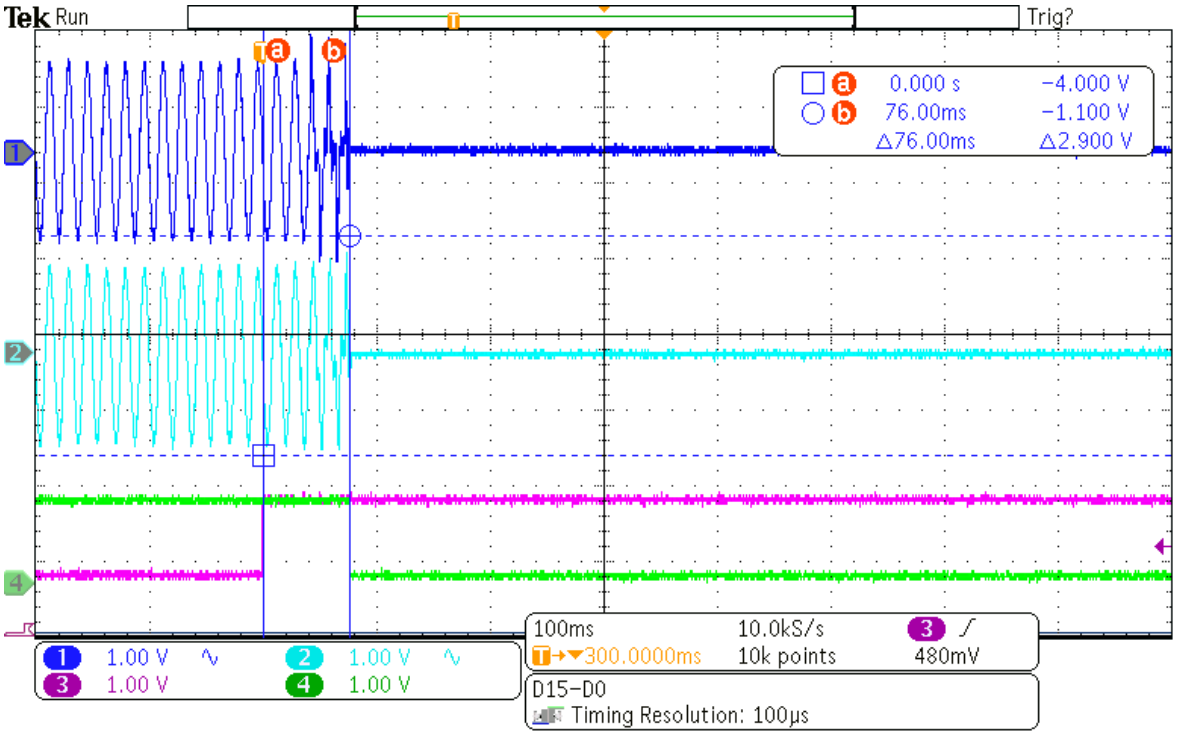
Source: Author.

Figure 5.38 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2 and 3: AFD.



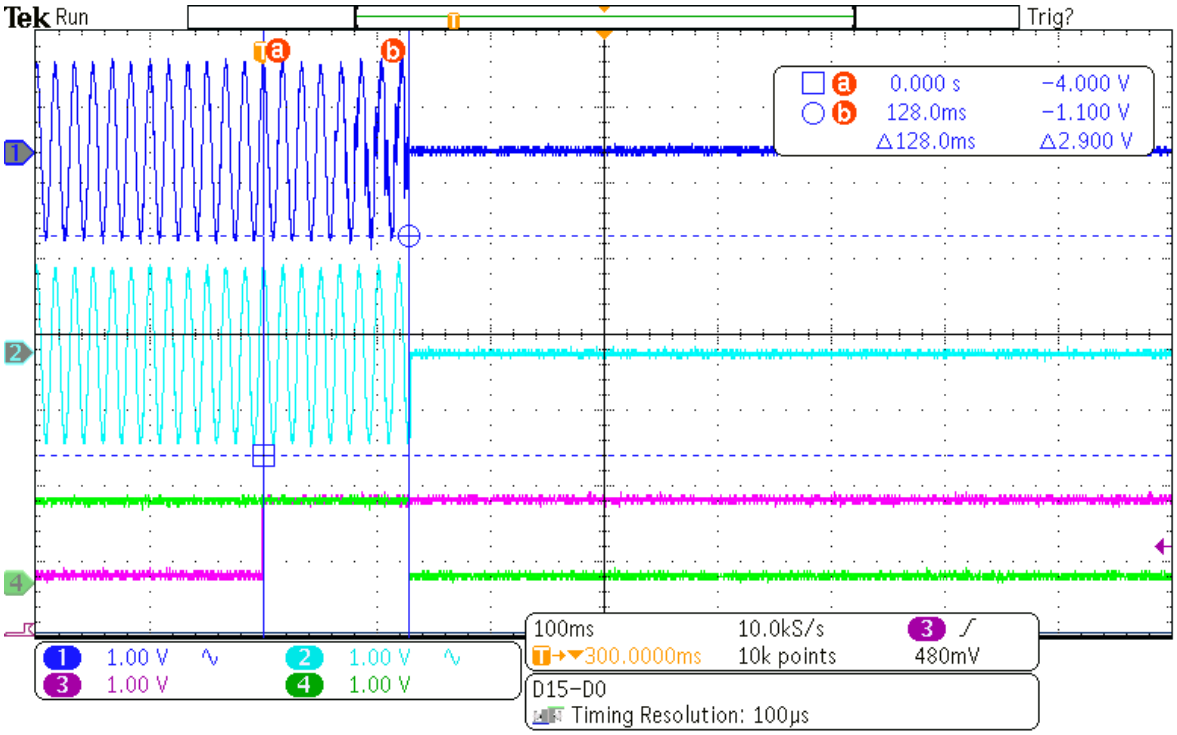
Source: Author.

Figure 5.39 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2 and 3: AFD by (CHEN et al., 2013).



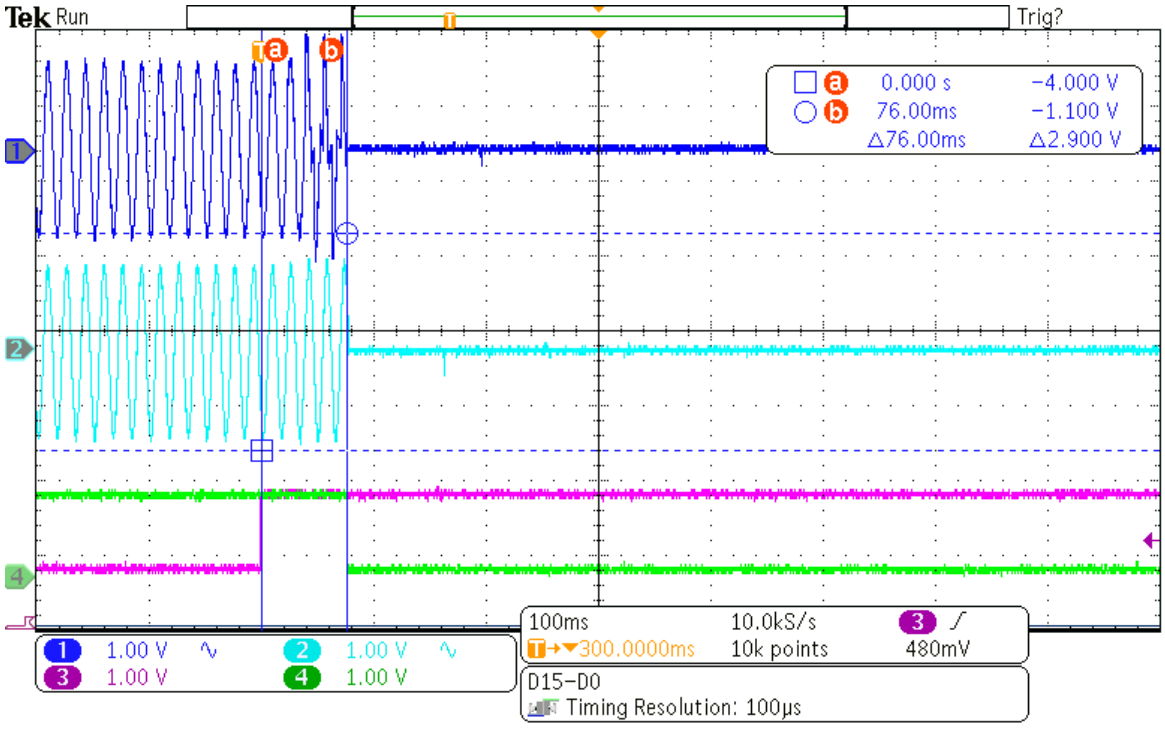
Source: Author.

Figure 5.40 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2 and 3: AFDPCF.



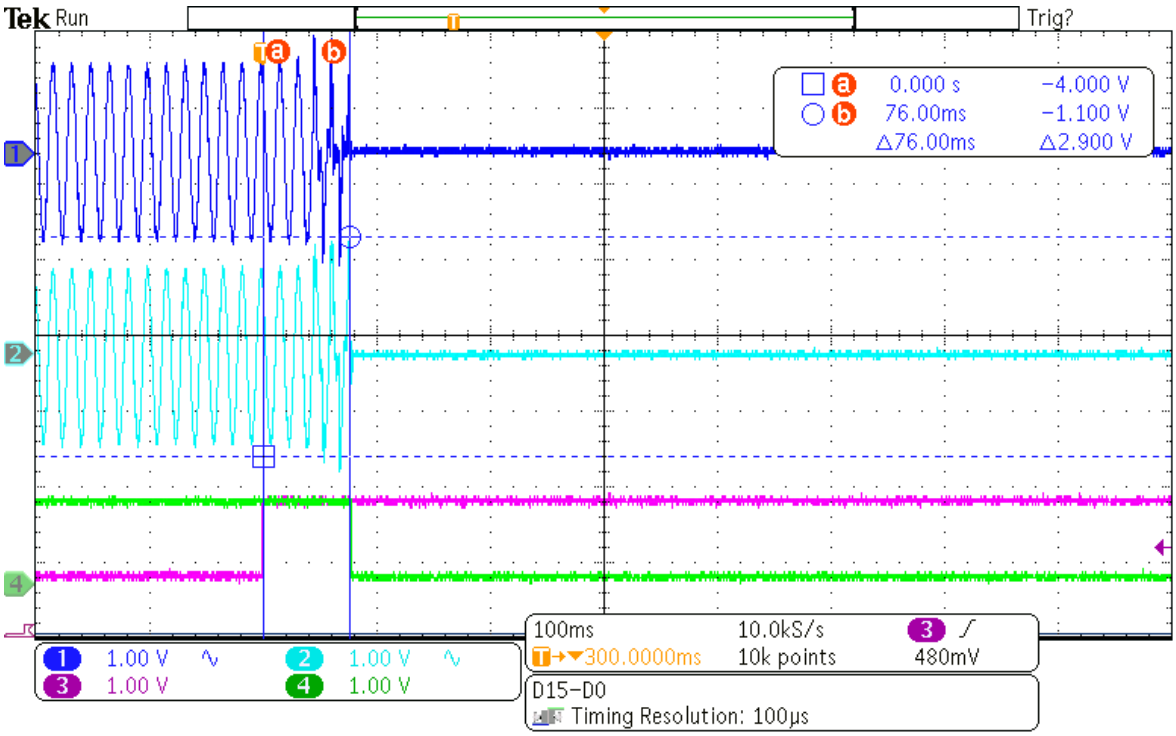
Source: Author.

Figure 5.41 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2 and 3: SFS.



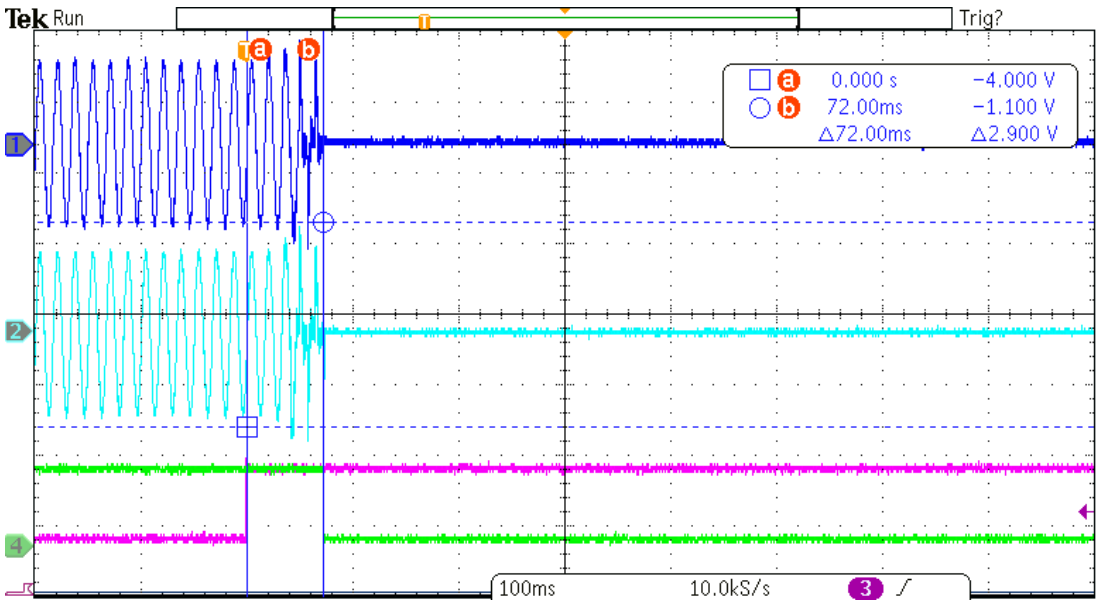
Source: Author.

Figure 5.42 – Islanding result for the combination Inverter 1: APJPFIP// Inverter 2 and 3: APJPF.



Source: Author.

Figure 5.43 – Islanding result for the combination Inverter 1, 2 and 3: APJPFIP.



Source: Author.

5.9.1 Time Detection Comparison.

The presented results confirm the effectiveness of the proposed solution when working in parallel with other known AIP methods. However, it is necessary to compare the detection times achieved when all inverters are equipped with APJPFIP to those achieved by these methods when working in a single DG environment. Figures 5.44, 5.45 and 5.46 demonstrate the results of detection time for $Q_f = 1$, $Q_f = 2.5$ and $Q_f = 5$.

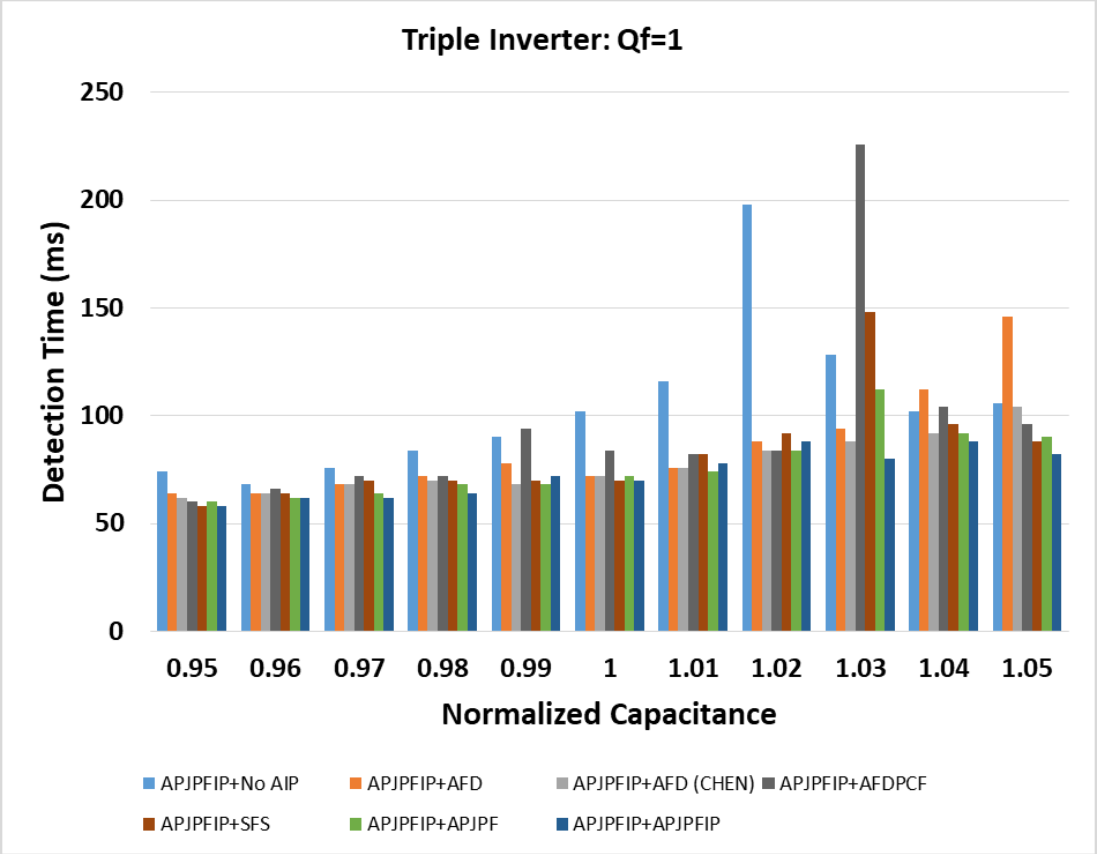
The main obtained results indicate the following:

- In the first combination, the inverter 1 was equipped with the proposed strategy and both other inverters will present only the passive AIP. No NDZ case was observed. The highest detection time was 304ms for the condition in which $Q_f = 5$ and C_{norm} =1.01. The average detection times were, respectively 107ms, 107ms and 126ms.
- In the second combination, the inverter 1 was equipped with the proposed strategy and both other inverters will present the AFD algorithm. One NDZ case was observed for $Q_f = 5$ and $C_{norm} = 1.02$. The highest detection time was 272ms for the condition in which $Q_f = 5$ and $C_{norm} = 1.03$. The average detection times were, respectively 85ms, 100ms and 124ms.
- In the third combination, the inverter 1 was equipped with the proposed strategy and both other inverters will present the AFD algorithm proposed by (CHEN et al., 2013).

No NDZ case was observed. The highest detection time was 1164ms for the condition in which $Q_f = 5$ and C_{norm} =1.02. The average detection times were, respectively 77ms, 107ms and 206ms.

- In the fourth combination, the inverter 1 was equipped with the proposed strategy and both other inverters will present the AFDPCF. No NDZ case was observed. The highest detection time was 278ms for the condition in which $Q_f = 5$ and $C_{norm} = 1.01$. The average detection times were, respectively 95ms, 108ms and 125ms.
- In the fifth combination, the inverter 1 will be equipped with the proposed strategy and both other inverters will present the SFS. No NDZ case was observed. The highest detection time was 278ms for the condition in which $Q_f = 5$ and $C_{norm} = 1.01$. The average detection times were, respectively 83ms, 101ms and 94.7ms.

Figure 5.44 – Comparison of the detection time for $Q_f = 1$ for triple inverter scenario.

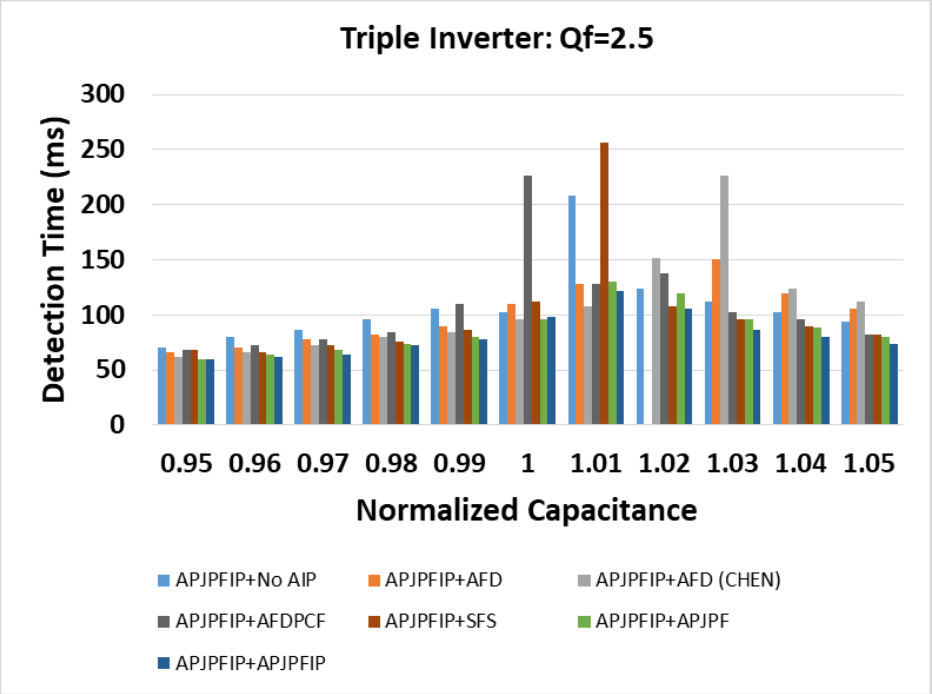


Source: Author.

- In the sixth combination, the inverter 1 was equipped with the proposed strategy and both other inverters will present the APJPF. No NDZ case was observed. The highest detection time was 218ms for the condition in which $Q_f = 5$ and $C_{norm} = 1.02$. The average detection times were, respectively 77ms, 87ms and 103ms.

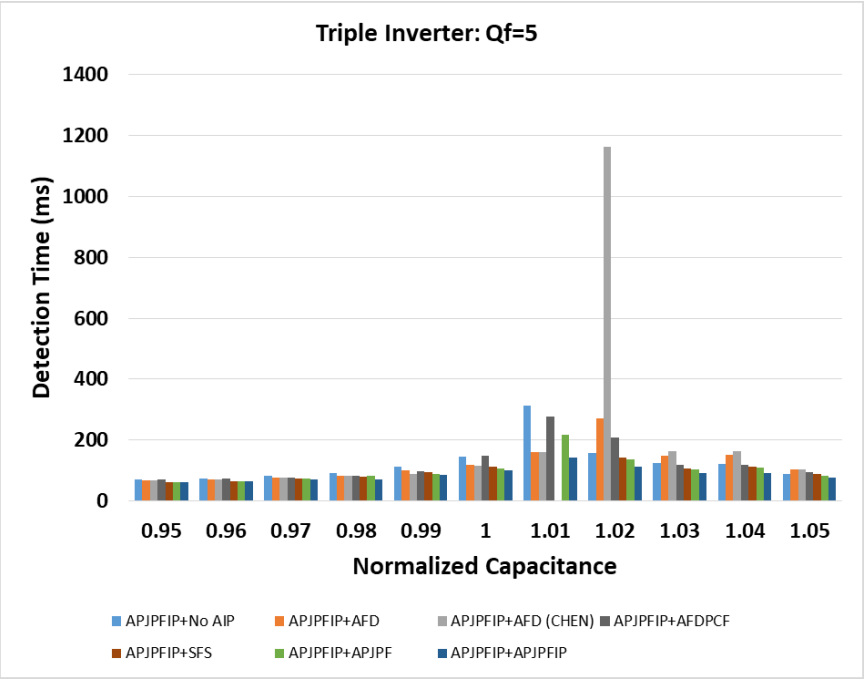
- In the seventh combination, all the inverters will be equipped with the proposed strategy. No NDZ case was observed. The highest detection time was 218ms for the condition in which $Q_f = 5$ and $C_{norm} = 1.02$. The average detection times were, respectively 77ms, 87ms and 103ms.

Figure 5.45 – Comparison of the detection time for $Q_f = 2.5$ for triple inverter scenario.



Source: Author.

Figure 5.46 – Comparison of the detection time for $Q_f = 5$ for triple inverter scenario.



Source: Author.

Finally, table 5.3 condenses all the obtained results for the double inverter scenario.

Table 5.3 – Detection time results for triple inverter environment.

Qf=1	***Cnorm***	***Methods***						
		APJPFIP	**APJPF**	**SFS**	**AFDPCF**	**AFD by Chen**	**AFD**	**No AIP**
	0.95	58	60	58	60	62	64	74
	0.96	62	62	64	66	64	64	68
	0.97	62	64	70	72	68	68	76
	0.98	64	68	70	72	70	72	84
	0.99	72	68	70	94	68	78	90
	1	72	76	76	128	76	79	113
	1.01	78	74	82	82	76	76	116
	1.02	88	84	92	84	84	88	198
	1.03	80	112	148	226	88	94	128
	1.04	88	92	96	104	92	112	102
	1.05	82	90	88	96	104	146	106
	Average	72	72	70	84	72	76	102
	NDZ Cases	0	0	0	0	0	0	0
	Cnorm	**APJPFIP**	**APJPF**	**SFS**	**AFDPCF**	**AFD by Chen**	**AFD**	**No AIP**
	0.95	60	60	68	68	62	66	70
	0.96	62	64	66	72	66	70	80
	0.97	64	68	72	78	72	78	86

	0.98	72	74	76	84	80	82	96
	0.99	78	80	86	110	84	90	106
	1	98	96	112	226	96	110	102
	1.01	122	130	256	128	108	128	208
	1.02	106	120	108	138	152	ndz	124
	1.03	86	96	96	102	226	150	112
	1.04	80	88	90	96	124	120	102
	1.05	74	80	82	82	112	106	94
	Average	78	80	86	96	96	98	102
	NDZ Cases	0	0	0	0	0	0	0
Qf=5	**Cnorm**	**Methods**						
		APJPFIP	**APJPF**	**SFS**	**AFDPCF**	**AFD by Chen**	**AFD**	**No AIP**
	0.95	61	63	63	71	69	67	71
	0.96	64	66	66	74	72	70	74
	0.97	70	74	74	76	78	78	82
	0.98	72	82	80	84	84	84	92
	0.99	86	90	96	98	90	102	112
	1	102	108	114	150	116	118	146
	1.01	144	218	NDZ	278	160	162	312
	1.02	112	136	142	208	1164	272	158
	1.03	92	104	108	120	164	150	124
	1.04	92	110	112	118	164	152	122
	1.05	76	82	88	94	104	104	90
	Average	86	90	88	98	104	104	112
	NDZ Cases	0	0	1	0	0	0	0

Source: Author.

5.10 Quadruple Inverter Islanding Results

This section aims to determine the performance of the analyzed AIP in a quadruple inverter-based DGS system in real-time. For this kind of environment, the proposed algorithm will be tested in four different conditions:

- Condition 1: Four inverters with the proposed algorithm.
- Condition 2: Three inverters will work with the APJPFIP algorithm and one of them with the passive AIP.
- Condition 3: Two inverters with the proposed method and two with no active AIP.
- Condition 4: One inverter with the APJPFIP method and the other three inverters with no active AIP.

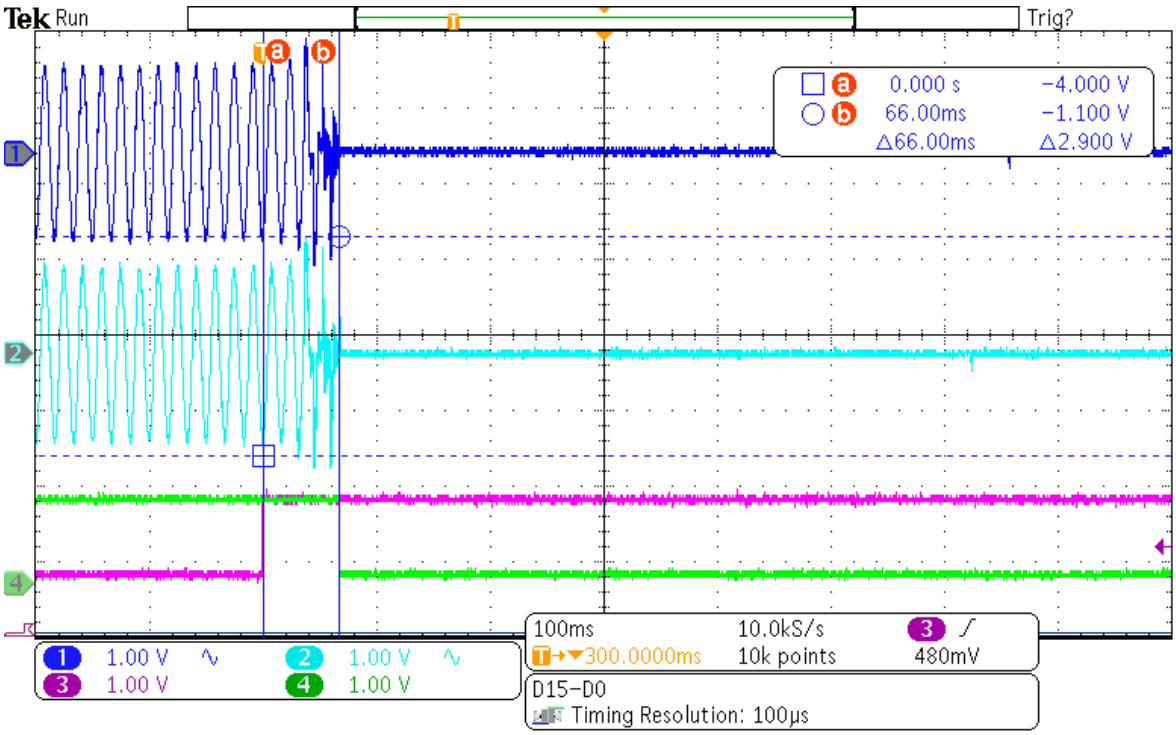
In this way, this subsection of results will test the proposed algorithm for a quadruple-based inverter system when it is responsible for 100%, 75%, 50% and 25% of the total active power generated.

5.10.1 Condition 1

Figure 5.47 shows the results of output current, islanding, and Trip signals during an unintentional islanding event for this configuration, considering both a unitary quality factor and normalized capacitance. This result refers to the condition in which the four inverters are working equipped with the proposed algorithm. Due to the oscilloscope's four-channel limitation, only two currents are displayed. The detection time recorded was 66 ms.

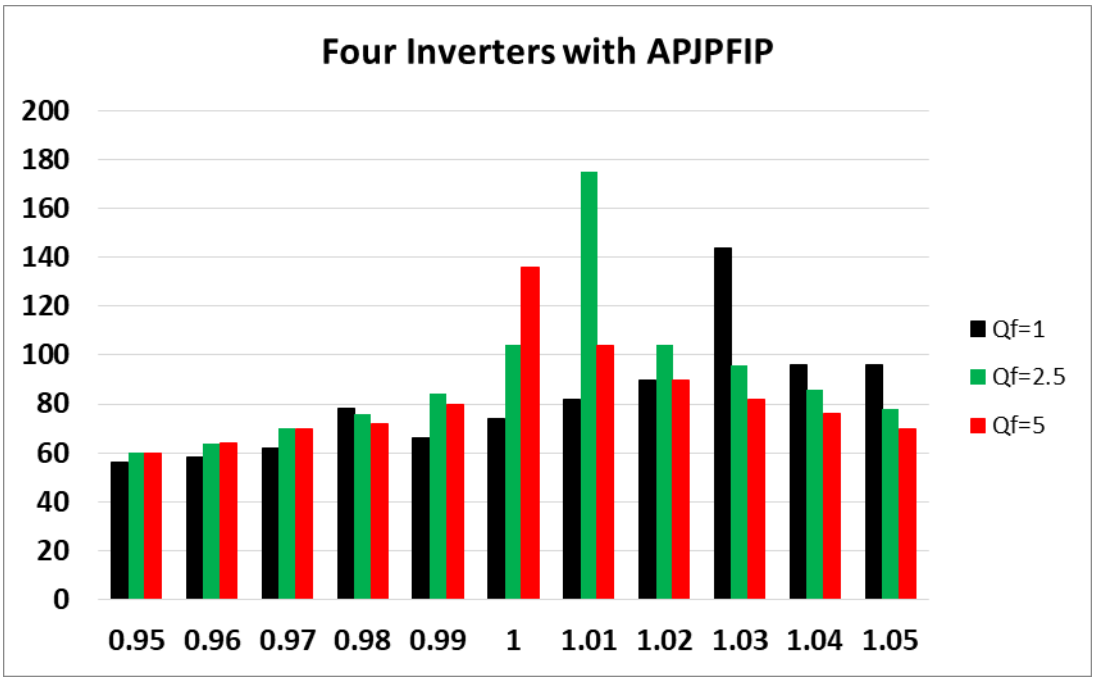
As can be seen in Figure 5.48, that illustrates all the obtained results for condition, the APJPFIP method was able to reach correct islanding detection for all the tested cases. The highest result was 175ms for the condition in which $Q_f = 5$ and $C_{norm} = 1.01$. The average detection times were, respectively 82ms, 82ms and 91ms.

Figure 5.47 – Islanding result for condition 1.



Source: Author.

Figure 5.48 – Condition 1 islanding results for three quality factors.



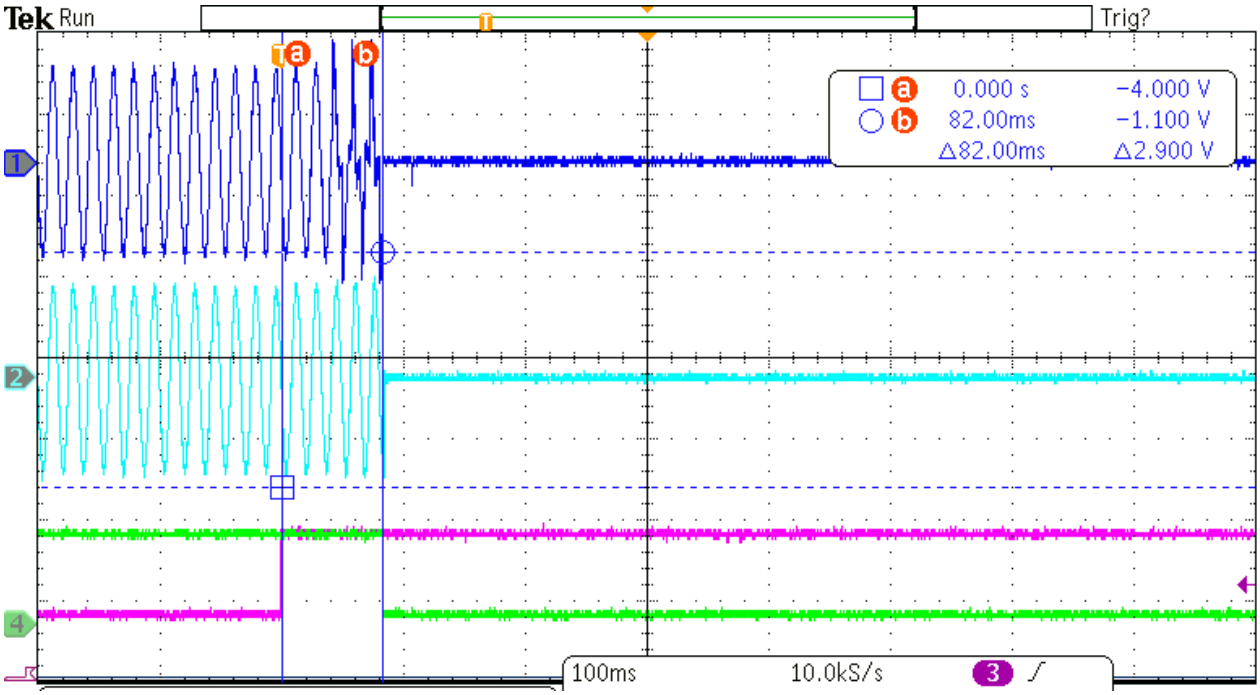
Source: Author.

5.10.2 Condition 2

Figure 5.49 demonstrates the results of output current Islanding and Trip signals for an unintentional islanding for this combination, for both unitary quality factor and normalized capacitance. This result refers to the condition in which the three inverters are working equipped with the proposed algorithm and the other inverter with no active AIP. The currents represented in this figure are the currents of inverter 1 (equipped with the APJPFIP) and of inverter 2 (equipped with no active AIP). The detection time was 82ms.

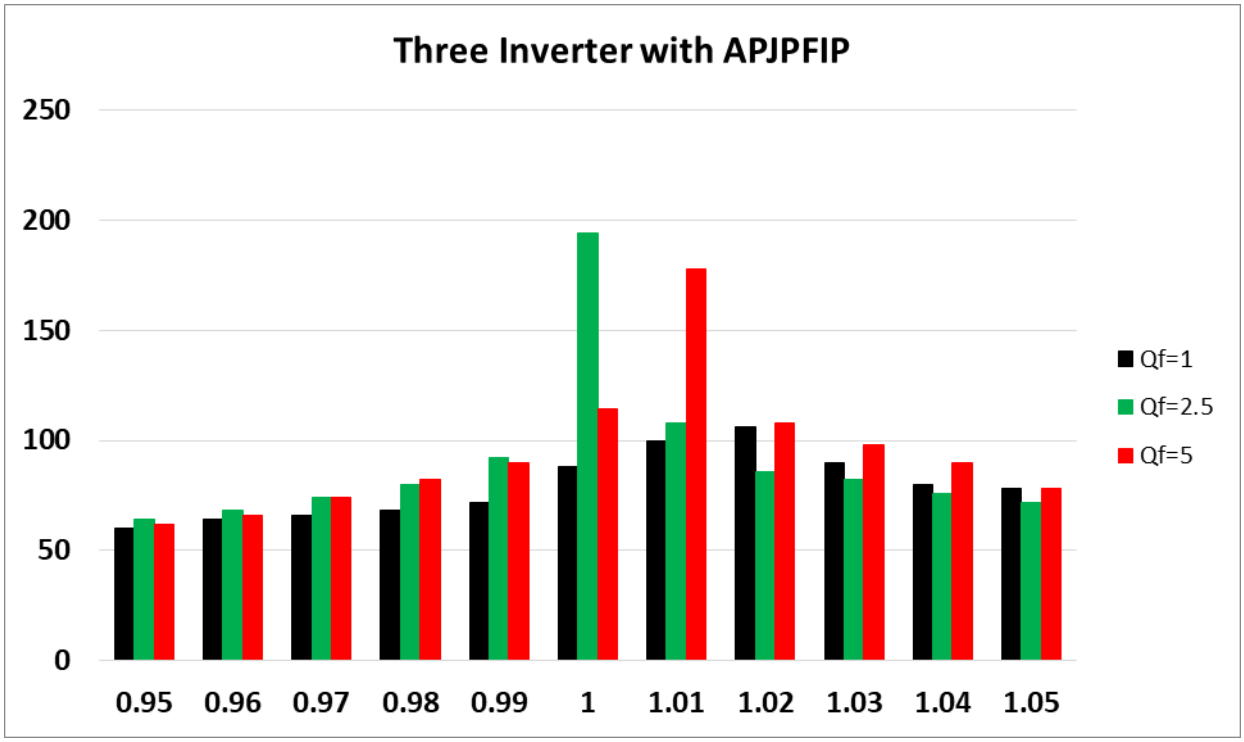
As can be seen in Figure 5.50, which illustrates all the obtained results for condition, the APJPFIP method was able to reach correct islanding detection for all the tested cases. The highest result was 178ms for the condition in which $Q_f = 5$ and $C_{norm} = 1.01$. The average detection times were, respectively 79ms, 91ms and 95ms.

Figure 5.49 – Islanding result for condition 2.



Source: Author.

Figure 5.50 – Condition 2 islanding results for three quality factors.



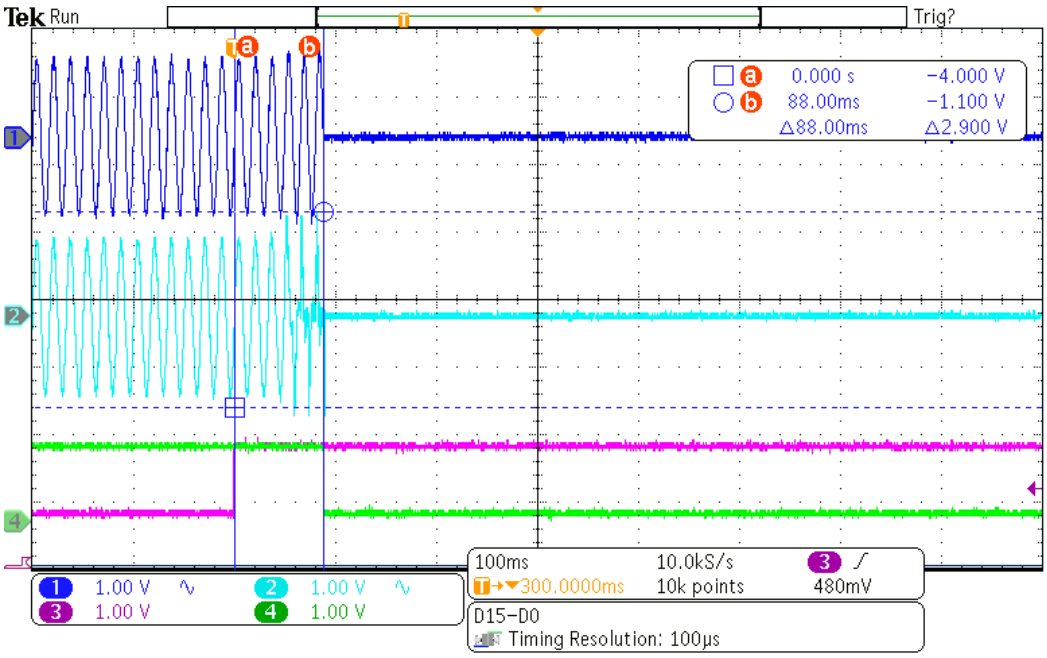
Source: Author.

5.10.3 Condition 3.

Figure 5.51 demonstrates the results of output current Islanding and Trip signals for an unintentional islanding for this condition, for both unitary quality factor and normalized capacitance. This result refers to the condition in which the two inverters are working equipped with the proposed algorithm and the other two inverter with no active AIP. The currents represented in this figure are the currents of inverter 1 (equipped with the APJPFIP) and of inverter 2 (equipped with no active AIP). The detection time was 88ms.

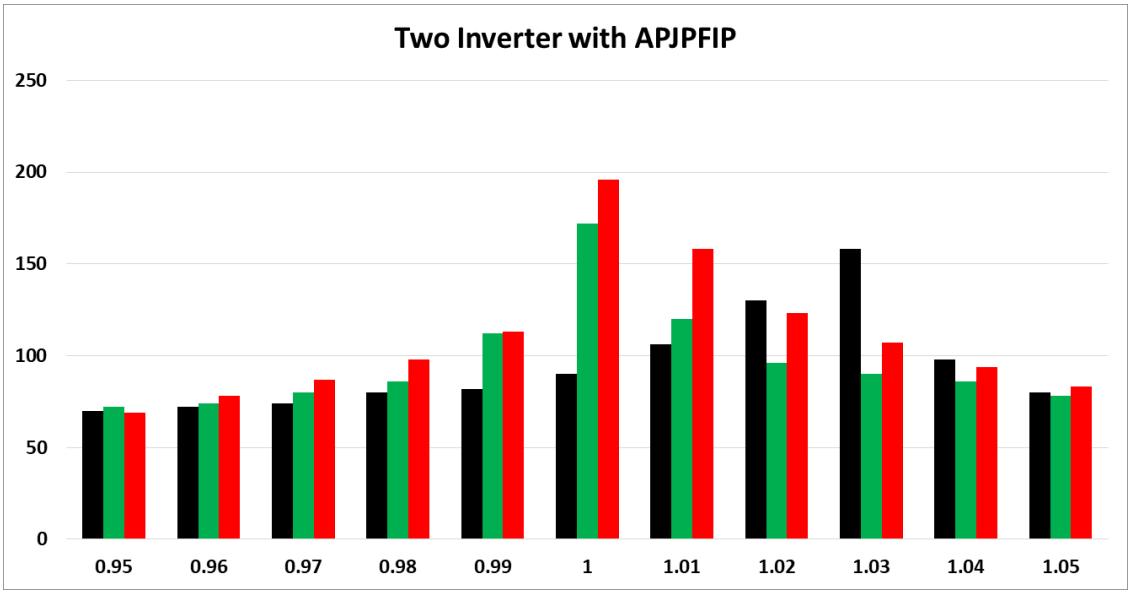
As can be seen in Figure 5.52, that illustrates all the obtained results for condition, the APJPFIP method was able to reach correct islanding detection for all the tested cases. The highest result was 178ms for the condition in which $Q_f = 5$ and $C_{norm} = 1.01$. The average detection times were, respectively 95ms, 97ms and 110ms. No NDZ case was verified.

Figure 5.51 – Islanding result for condition 3.



Source: Author.

Figure 5.52 – Condition 3 islanding results for three quality factors.

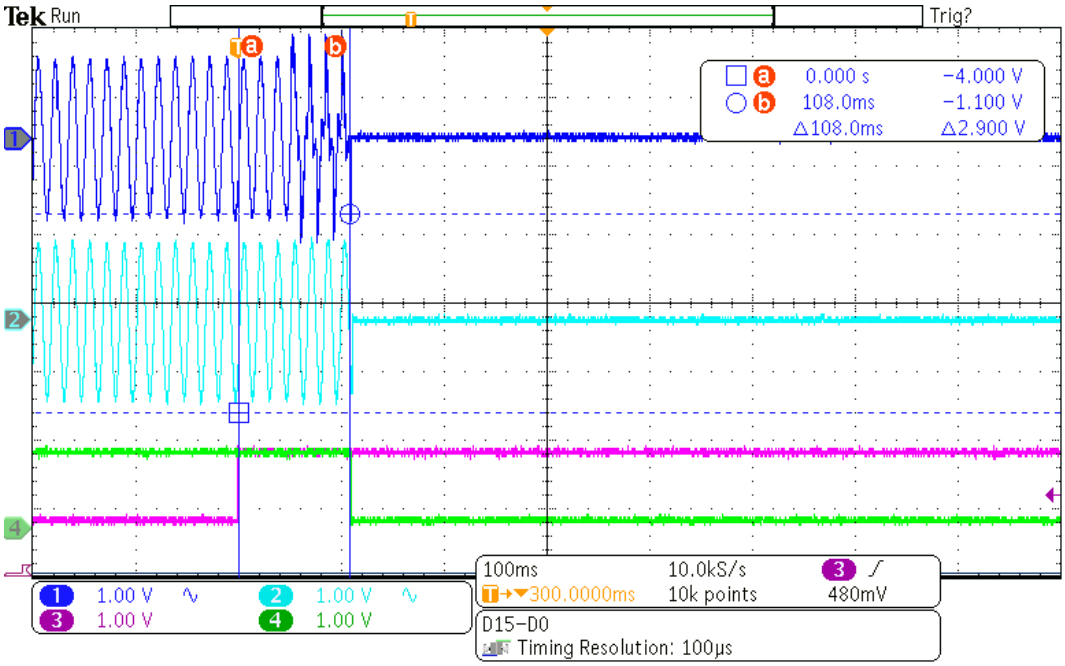


Source: Author.

5.10.4 Condition 4.

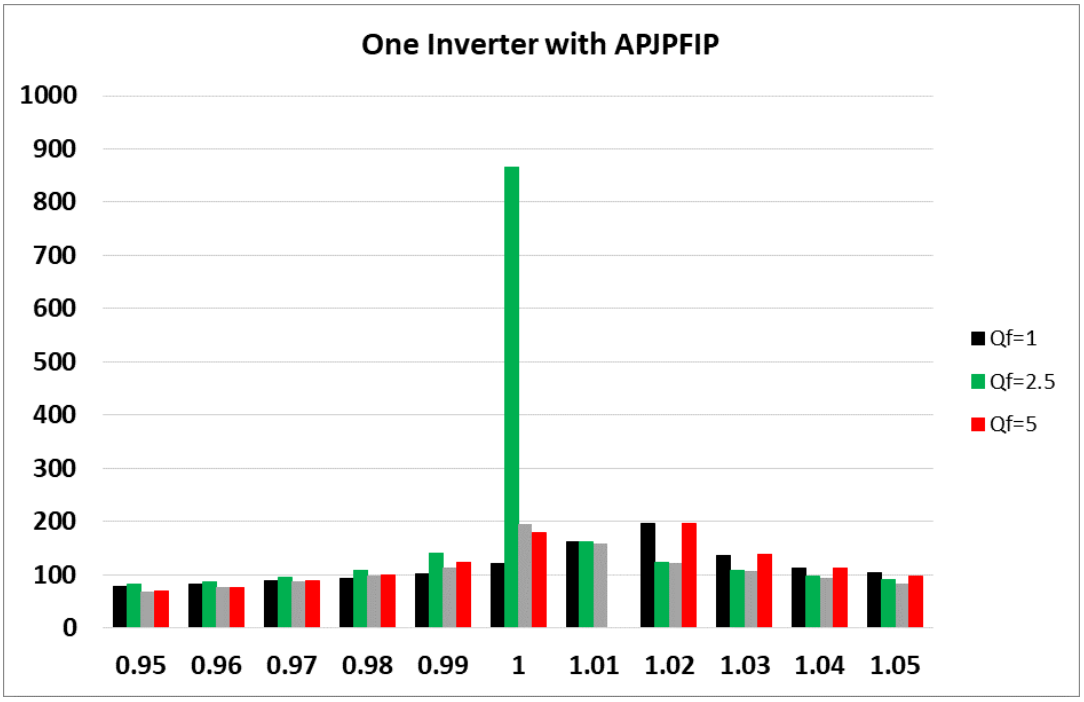
Figure 5.53 demonstrates the results of output current Islanding and Trip signals for an unintentional islanding for this condition, for both unitary quality factor and normalized capacitance. The currents represented in this figure are the currents of inverter 1 (equipped with the APJPFIP) and of inverter 2 (equipped with no active AIP). The detection time was 108ms. As can be seen in Figure 5.54, that illustrates all the obtained results for condition, the APJPFIP method was able to reach correct islanding detection for all the tested cases. The highest result was 866ms for the condition in which $Q_f = 2.5$ and $C_{norm} = 1$. The average detection times were, respectively 116ms, 178ms and 118ms.

Figure 5.53 – Islanding result for condition 3.



Source: Author.

Figure 5.54 – Condition 3 islanding results for three quality factors.



Source: Author.

5.11 Final Considerations

This chapter compared the real time performance of the proposed scheme in comparison with the other implemented active AIP methods: AFD, AFD by (CHEN et al., 2013), AFDPCF, SFS and APJPF. It presented the adopted setup and the configuration of the system emulated in the Typhoon Hil device.

In relation to the THDi, the Classic AFD obtained the worst qualitative performance, increasing the THDi from 2.32% to 4.93%, reaching the boundaries of the Standards threshold for power quality. The harmonic content generated by the AFDPCF was 3.01% and, therefore, the method reached the second worst performance. The SFS algorithm reached 2.85%, AFDPCF and APJPF reached 2.5%. The best THDi result, finally, was reached by the proposed method. This fact, in turn, shows the advantages of the intermittent perturbation of the θ_{Z_o} parameter that improves the islanding detection capabilities without the increasing of the harmonic content of the inverter output current.

Regarding the detection time, the methods were submitted to islanding occurrences in single and multi-inverter scenarios. In the first step, a single inverter was connected to a RLC load and the main grid. Each method was submitted to a battery of 33 tests for different values of normalized capacitance and quality factor. The proposed method was the only one that did not incur in any NDZ case and achieved lower detection time for all the tested conditions.

Once it was proved the good performance of the proposed method in comparison to the other well-knonw solutions, the second step of the work was to demonstrate the capability of the proposed solution to work in parallel with other methods present in literature. The method was successfully tested in a double and triple inverter based distributed generation system, reaching correct islanding detection in parallel with the other methods. Finally, the method was tested in a quadruple inverter based DG, assuming 100%, 75%, 50%, and 25% of the total generated power, reaching no NDZ case and accomplishing islanding detection in less than 1 second for all the tested conditions.

The results obtained demonstrate the proposed solution can be successful applied within a microgrid context due to its adaptability and reliability. The method proved to be effective when integrated into a multi-inverter based DGS, maintaining consistent detection performance even under adverse load conditions. Furthermore, the method exhibited compatibility with other established anti-islanding techniques, operating seamlessly in parallel without compromising

accuracy or efficiency. These findings suggest that the method can be reliably deployed in modern microgrids, ensuring robust islanding detection while supporting diverse DG sources.

CHAPTER VI

Conclusions

6.1 Conclusion

This work presented, in general terms, the main motivations for the adoption of renewable energy sources in detriment of fossil fuels. The main reasons cited were: the mitigation of the global warming effects, job creations and reduction of the water-based generation systems. Beyond that, it was highlighted the importance of the reducing the demand for large electricity generation centers by the popularization of the DGS's. However, in spite of all the advantages, the growing penetration of the DGS into the utility grid generates a series of problems that must be addressed by the academical research. Therefore, it is important to study the basis of the islanding phenomenon in order to develop accurate solutions to eliminate the negative consequences of this contingency.

The second chapter, in turn, introduced information about the mandatory GTPS topics in order to facilitate the total comprehension about the islanding theory and the performance of the AIP solutions. It covered the PLL algorithms, highlighting the SOGI PLL, once it was chosen to perform the inverter synchronization during the computational tests in virtue of its low oscillations of the measured frequency. Posteriorly, it was conducted a summarization of the main Standards about the connection of the GTPS into the main utility grid. The mentioned Standards were: IEEE 929-2000, IEEE 1547-2003, ABNT NBR 16149 and ABNT NBR IEC 62116.

The third chapter presented a review of the main passive and active approaches to perform the islanding detection. The passive strategies highlighted in the text were: OUF/OUV, phase jump monitoring, harmonic detection, ROCOF and other solutions based on the measuring of the rate of change of different electrical variables. The active solutions cited on the text were: AFD, IAFD, harmonic insertion, APJPF. It also covered the advantages and drawbacks of each strategy and the chapter conducted a detailed review of the modifications each solution suffered during the past years in order to guarantee more accuracy and efficiency on loss of mains detection. Finally, the last subsection of this chapter was dedicated to present the AIP by this work.

The fourth chapter presented the block diagrams of the power and control structures used during the AIP computational tests, the test methodology and the obtained results for islanding events in two environments: single and double inverter-based DGS. The proposed AIP scheme was compared to other well-known strategies and reached superior results in terms of NDZ, THDi and detection time for all of the analyzed conditions. Beyond that, it was the only technique able to perform the loss of mains detection for a load with quality factor equals to five.

Chapter V showed the real time implementation of a distributed energy system with four inverters conneted to the utility grid and to a RLC load. The RLC load was tuned according the main grid code recommendations. However, its parameters were adjustable to reach different values of quality factor and normalized capacitance. The results of THDi showed the proposed method is the less intrusive in relation of power quality. In this sense, it was responsible for increasing the harmonic content of the output current inverter from 2.32 to 2.41%.

In relation to islanding detection itself the proposed solution was compared with AFD, AFD by (CHEN et al, 2013), AFDPCF, SFS and APJPF in a single inverter DGS. It were performed tests for different values of quality factor and normalized capacitance and the proposed method was not only the fastest but also the only one that reached correct detection for all the tests. Moreover, the APJPFIP capability to work in parallel with other solutions in a multi-DG environment. It performed correct islanding detection for a double, triple and quadruple inverter based DGS.

The obtained results indicate that the proposed solution can be effectively implemented in a microgrid environment, thanks to its adaptability and reliability. The method demonstrated strong performance when applied to a multi-inverter distributed generation system (DGS), consistently detecting islanding even under challenging load conditions. Additionally, it was found to work well alongside other established anti-islanding methods, running in parallel without sacrificing accuracy or efficiency. These outcomes suggest that the method is well-suited for deployment in contemporary microgrids, offering reliable islanding detection while accommodating various DG sources.

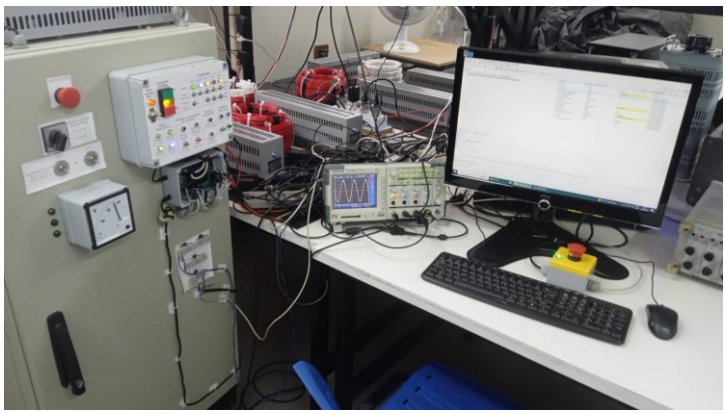
6.2 Future Works

This text presented a new AIP algorithm called APJPFIP. Through offline simulation and real time implementation, this work concluded the effectiveness of the algorithm in terms of

power quality, detection time and capability to work in parallel with other strategies. However, in order to continue the timeline evolution of the proposed method, some tasks have to be done. Those tasks, in turn, are related to hardware implementation, selectivity studies and other general improvements.

In relation to hardware implementation, it is important to state that three inverter units are in process of manufacturing. One of the units is shown in Figures 6.1 and 6.2. The power structure is composed by a three-phase full bridge based inverter and the filtering of the output current presents a LCL configuration. The controlling code can be embedded in a TMS320F28335 from Texas Instruments ®.

Figure 6.1 – Inverter unit operating.



Source: Author.

Figure 6.2 – Inverter unit inside.

Source: Author.

Beyond that, it is important to understand the capabilities of the proposed algorithm fo distinguishing islanding and non-islanding contigences. Studies will be carried out to determine the performance of the proposed method after natural contigences as motor starting, capacitor bank switching and non-linear loads. Finally, some improvements can be done linking the method with the monitoring of passive features such as THDi or ROCOF.

Summarizing, the next steps of this work should focus on:

- Prototyping of inverters for testing the proposed method in a physical power plant;
- Testing of the proposed method performance for three-phase inverters;
- Testing the proposed method selectiveness capabilities through non-islanding events;
- Improve the proposed method by including monitoring of other passive features;
- Testing the proposal algorithm in a microgrid environment.

6.3 Publications to Date

It is important to highlight that this work led to three major publications on anti-islanding methods for inverter based distributed energy resources. The first presents the APJPF algorithm, the second provides a comparative analysis between the APJPF method and other strategies in the literature, and the third is a comprehensive review of AIP schemes and their timeline of development. There is also a filed patent application related to the proposed method. Beyond that, the author collaborated on research projects with the School of Technology and Innovations at the University of Vaasa under the supervision of Professor Marcelo Godoy Simões. These projects included applying artificial neural networks for inverter control and model predictive control for autonomous microgrids. Lastly, the author also contributed to doctoral research on MPPT techniques conducted at the Federal University of Uberlândia.

Publications on anti-islanding techniques for inverter based DGS:

- RESENDE, Ê. C. et al. Proposta de uma nova estratégia ativa de anti-ilhamento baseada em realimentação positiva de frequência. *Brazilian Journal of Power Electronics*, v. 26, n. 3, p. 302–314, 2021. https://doi.org/10.18618/REP.2021.3.0007

- RESENDE, Ê. C. et al. Implementation and Critical Analysis of the Active Phase Jump with Positive Feedback Anti-Islanding Algorithm. 2022. https://doi.org/10.3390/en15134609

- RESENDE, E. C;, SIMÕES, M. G.; FREITAS, LCG. Anti-Islanding Techniques for Integration of Inverter-Based Distributed Energy Resources to the Electric Power System. IEEE Access, vol. 12, pp. 17195-17230, 2024. https://doi.org/10.1109/ACCESS.2024.3357710

Filed Patent Application on Anti-Islanding Protection:

- RESENDE, E. C.; Freitas, L. C. G., METHOD FOR ANTI-ISLANDING DETECTION IN DISTRIBUTED GENERATION SYSTEMS AND MICROGRIDS. 2023, Brazil. Patent: Innovation Privilege. Registration number: BR1020230060536, title: "METHOD FOR ANTI-ISLANDING DETECTION IN DISTRIBUTED GENERATION SYSTEMS AND MICROGRIDS," Registration Institution: INPI - National Institute of Industrial Property. Filed: 03/31/2023; Examination Request: 10/04/2024. Funding Institutions: CNPq, FAPEMIG, and CAPES. Available at: https://revistas.inpi.gov.br/rpi/ (Industrial Property Journal, SECTION VI PATENTS, No. 2804, October 1, 2024).

Publications in partnership with research groups from the School of Technology and Innovations at the University of Vaasa:

- Q. Ullah, P. Razmi, Ê. Costa Resende and M. G. Simões, "Analyzing the Performance of AC Microgrids in Stand-Alone Operation with Artificial Neural Network Controllers," 2024 International Workshop on Artificial Intelligence and Machine Learning for Energy Transformation (AIE), Vaasa, Finland, 2024, pp. 1-6, doi: 10.1109/AIE61866.2024.10561255.
- ULLAH, QUDRAT; RESENDE, E. C.; FREITAS, LUIZ CARLOS GOMES; LAAKSONEN, H.; SIMOES, MARCELO GODOY. Enhancing Voltage Stability of Grid-Forming Power Converters Based on Model Predictive Control. International Journal Of Electrical Power & Energy Systems. (Accepted for publication)

Publications in partnership with researches of Federal University of Uberlandia:

- P. A. R. Freitas *et al*., "New Global Maximum Power Point Tracking Technique Based on Indirect PV Array Voltage Control for Photovoltaic String Inverters With Reduced Number of Sensors," in *IEEE Access*, vol. 12, pp. 43495-43505, 2024, doi: 10.1109/ACCESS.2024.3380475.

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